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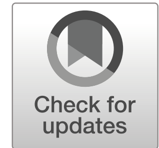


# A Comparative Study on Scaling Capabilities of Si and SiGe Nanoscale Double Gate Tunneling FETs

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**Abstract**

In the last few years, an accelerated trend towards the miniaturization of nanoscale circuits has been recorded. In this context, the Tunneling Field-Effect Transistors (TFETs) are gaining attention because of their good subthreshold characteristics, high scalability and low leakage current. However, they suffer from low values of the ON-state current and severe ambipolar transport mechanism. The aim of this work is to investigate the performance of SiGe nanoscale Double Gate TFET device including low doped drain region. The electrical performance of the considered device is investigated numerically using ATLAS 2D simulator, where both scaling and reliability aspects of the proposed design are reported. In this context, we address the impact of the channel length, traps density and drain doping parameters on the variation of some figures of merit of the device namely the swing factor and the $I_{ON}/I_{OFF}$ ratio. The obtained results indicate the superior immunity of the proposed design against traps induced degradation in comparison to the conventional TFET structure. Therefore, this work can offer more insights regarding the benefit of adopting channel materials and drain doping engineering techniques for future reliable low-power nanoscale electronic applications.

**Keywords** TFET design · SiGe alloy · Scaling · Interface traps

## 1 Introduction

Today, the electronics industry is the subject of significant changes with the aim of increasing both density and speed of integrated circuits. Roughly speaking, the boost of circuit performances is tightly linked to the downscaling of elementary components. The scaling trend can be expressed by the rule of two, which states that between two generations of technology, the device feature size is decreased by two while some other criteria such as energy dissipation is increased similarly by a factor of two [1]. In fact, the accelerated shrinking of metal-oxide semiconductor field-effect transistor is accompanied by proposition and testing of innovative technologies in order to extend CMOS to the deep nanoscale level. Hence, research efforts should be accentuated on two principle features: one concerns scaling CMOS under sever manufacturing constraints and the other deals with new approaches for information treatment to maintain operating miniaturization beyond the domain of CMOS [2].

The amount of power consumed by digital circuits has become a major concern since they are based on MOSFET devices. As a matter of fact, the drain induced barrier lowering associated with transistors is more pronounced at the nanoscale level. This can induce the Off-state leakage current increase leading to enlarge the power consumption of nanoelectronic circuits. As a result, the aforementioned constraints prohibit the adoption of MOSFET devices for a wide range of applications [3]. In this context, attempts have been experienced so far to enhance the transistor by using various structures based on multi-gate designs [4–8]. Although these novel designs have enabled improved leakage performance and enhanced switching characteristics, more improvements remains of vital significance in order to push the scaling limits of CMOS-based technology.

The tunneling field-effect transistor has emerged as a promising device to deal with the downscaling challenges. This is because of its ability to deliver swing factor values less than

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the nominal value (60 mV/decade). Going beyond this threshold value is the result of the current control mechanism in comparison to the conventional MOSFETs. In other words, the current in a MOSFET device is basically governed by the drift-diffusion mechanism; while the TFET derived current depends on the band to band tunneling effect. This enables achieving small swing switch devices with low leakage power, which opens up a new path toward designing high-performance nanoelectronic circuits [9–12]. Furthermore, TFET devices display higher immunity against the short channel effects, which constitutes another paramount advantage with respect to conventional MOSFETs [11–13]. However, TFET-based designs still suffer from the low derived current capability and the ambipolarity problems. Thus, the deep knowledge of the conduction mechanism and the main reasons behind the device ambipolarity behavior is an essential issue to identify the appropriate design that enables improving the TFET device performance.

Despite that the Si based devices have attracted much attention in comparison to other materials, the SiGe alloy remains of large interest due to many benefits. The SiGe band gap can be adjusted by selecting the appropriate Ge content in the alloy, where it can be considered as a Si material in case of relatively high Ge molar fraction (less than 40%) [14]. As a result, the adoption of the SiGe alloy as a channel for the TFET device not only enables modulating the tunneling barrier but also allows boosting the carriers' mobility, which eventually leads to improve some performance criteria [15]. Accordingly, our aim in this work is to investigate both scaling and reliability capabilities of SiGe DG TFET with low drain doping at the nanoscale level. Indeed, the decrease of the drain doping broadens the depletion width within source-drain tunneling path, which significantly reduces the subthreshold current but with less influence on the ON-current. As a result, the $I_{ON}/I_{OFF}$ ratio and the swing factor are both enhanced. In addition, by lightly doping the drain side, we can efficiently remedy the ambipolar effect due to the increase of the tunneling distance from the channel valence band to the drain conduction band [16]. Due to the difficulty of elaborating mathematical compact models, we develop a numerical simulation framework using ATLAS 2D simulator in order to account for parasitic mechanisms such as short channel and quantum confinement effects. The assessment of the device reveals that it provides significant improvements over the conventional design in terms of immunity against short channel, interface traps and ambipolarity effects.

The rest of this paper is structured as follows. In Section 2, we provide a detailed depiction of the investigated TFET device. Section 3 presents the main results obtained for the SiGe DG TFET in comparison to the conventional silicon based device. Finally, the paper is achieved by Section 4, where basic findings in addition to some future perspectives are showcased.

## 2 Numerical Simulations

Figure 1 shows 3D schematics of the investigated designs, where Fig. 1(a) depicts the conventional Si-based DG TFET and Fig. 1(b) illustrates the proposed design with SiGe alloy. In comparison to the conventional DG TFET device, it can be noticed that the proposed design presents the following features. The SiGe alloy is adopted as the channel material instead of silicon. Furthermore, it is assumed that the drain extension region possesses a reduced doping with respect to the source extension region. For both devices, gates are placed in a symmetric manner on opposite sides of the channel, where the employed gate dielectric is formed by $SiO_2$.

The set of values associated to different geometrical and electrical configuration parameters adopted during the numerical simulation procedure is recapitulated in Table 1.

The numerical simulations are performed at room temperature (300 K) using ATLAS 2D simulator. Several physical models are activated in order to account for various transport and interaction mechanisms predominant for TFET structures at the nanoscale level [17]. The mobility of carriers in the channel is basically altered by various scattering phenomena. The inversion layer model proposed by Lombardi et al. can be activated by setting CVT in the Models statement in order to account for transverse field, doping and temperature. The SRH parameter is used to express the Shockley-Read-Hall recombination process occurring due to the existence of a trap within the forbidden gap of SiGe. Another important non radiative mechanism is AUGER recombination, where the excess energy is being released in the form of phonons through the contribution of three carriers. Such effect is pronounced in indirect band gap semiconductors such as silicon. In order to support high field velocity saturation related to parallel electric field, FLDMOB model is introduced. We adopt the density gradient model based on the moments of the Wigner function equations of motions in order to consider the effects due to the confinement of carriers. The band-gap narrowing effects are activated by defining the BGN parameter, where such effects are pronounced for highly doped regions.

As a matter of fact, Tunnel FET is highly suitable to low-power applications due to its extremely low off-state current and superb swing characteristics below the 60 mV/dec, which is the main limitation associated with FETs driven by drift-diffusion mechanism. In this framework, the band-to-band tunneling model available in SILVACO software is used to investigate the TFET-based transistor, while for the conventional MOSFET-based designs, the transport mechanism is governed by the drift-diffusion model [18–20].

For the electrostatic behavior modeling of the proposed nanoscale SiGe DG TFET, the tunneling transport mechanism is included using the nonlocal-BTBT command in

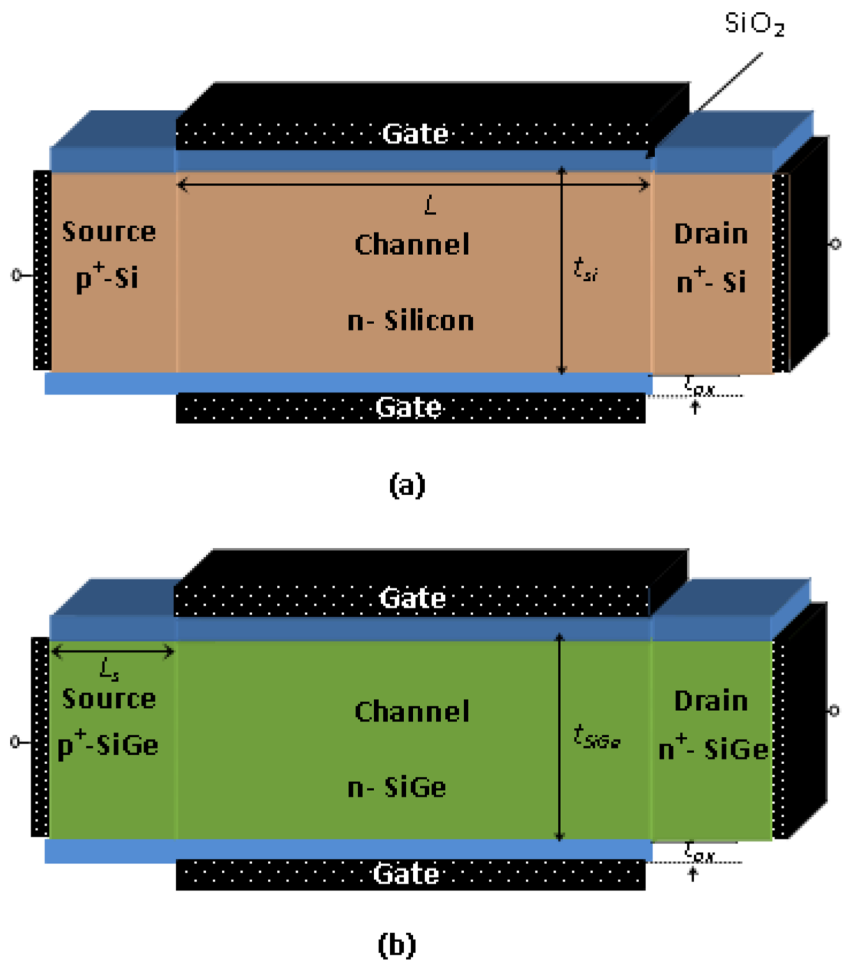



**Fig. 1** Two dimensional view of the investigated nanoscale DG TFET devices based on **a** Si material and **b** SiGe alloy

the models statement. This commend allows taking into account the nonlocal band to-band quantum tunneling model [11, 12]. The latter model indicates that the tunnel current is characterized by electrons and holes transfer across Source/Channel junction in which the tunnel barrier plays a crucial role in determining the drain current. It is worthy to mention that the current in the non-local BTBT model is related to the band edge profile. More accurately, the electric field varies dynamically at each point in the tunneling path rendering the tunneling a non-local process. Therefore, the tunnel current associated with an electron with longitudinal energy E and transverse energy $E_T$ can be given by the following equation [11, 12, 17].

$$J(E) = \frac{q}{\pi h}\iint T(E)[f_l(E+E_T) - f_r(E+E_T)]\frac{\sqrt{m_e m_h}}{2\pi h^2} dE dE_T \quad (1)$$

with $T(E)$ denotes the electrons tunneling probability, $m_e$ and $m_h$ represent respectively the effective electrons and holes masses, $q$ is the electron charge, $h$ refers to the Plank constant, $f_l$ and $f_r$ denote respectively the Fermi-Dirac functions on the left and the right sides of the Source/Channel junction and can be expressed as follows

$$\begin{cases} f_l(E) = \left(1+\exp\left[\left(E+E_T - E_{fSiGe}\right)/KT\right]\right)^{-1} \\ f_r(E) = \left(1+\exp\left[\left(E+E_T - E_{cfSiGe}\right)/KT\right]\right)^{-1} \end{cases} \quad (2)$$

where K is the Boltzmann constant, T denotes the temperature and $E_{fSiGe}$ represents Fermi level at the SiGe source region, while $E_{cfSiGe}$ is the Fermi level associated with the channel region.

**Table 1** Summary of values associated to configuration parameters during the numerical simulation

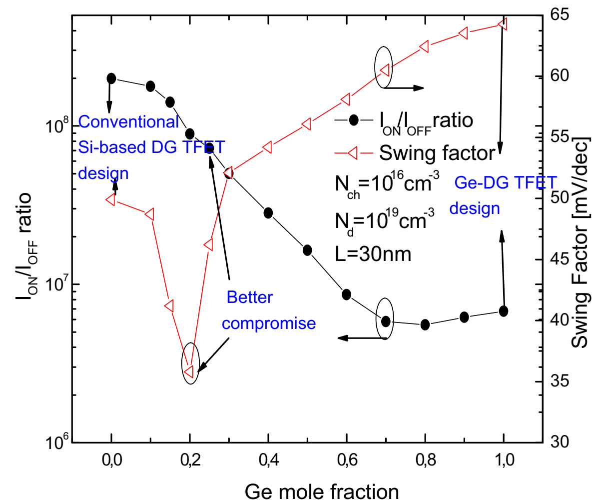
| Parameter | Notation | Value |
|---|---|---|
| Source/drain length | $L_{S/D}$ | 10 nm |
| Channel doping | $N_{Ch}$ | $10^{16}$ cm$^{-3}$ |
| Source region doping | $N_s$ | $10^{20}$ cm$^{-3}$ |
| Channel thickness | $t_{SiGe}$ | 5 nm |
| Oxide thickness | $t_{SiO2}$ | 1.5 nm |
| Gate workfunction | $Ø_{MS}$ | 4.6 eV |

In order to study the reliability characteristics of the proposed SiGe DG TFET-based device, hot carrier injection model is also involved. The latter model is considered extremely important at the nanoscale level, where the high electric field at the drain side induces interface traps affecting the device electrical behavior [21, 22]. Therefore, incorporating this model allows investigating the device degradation related to hot carrier injection effects and enables reproducing the realistic behavior of the investigated TFET design.

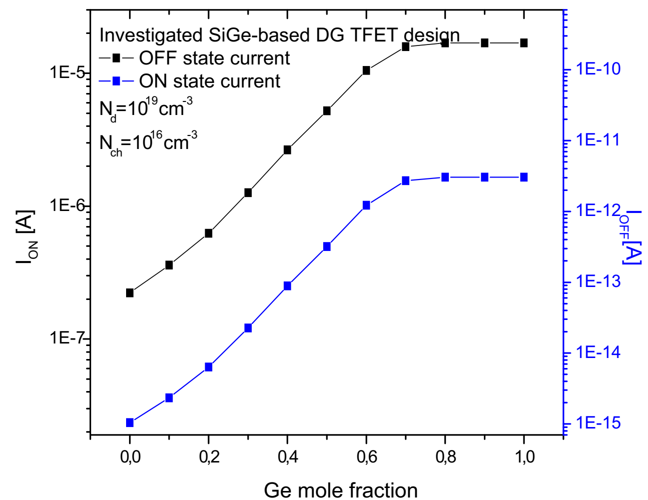
## 3 Results and Discussion

In this section, we analyze the performance of the proposed SiGe based device in comparison with its counterpart elaborated on a pure silicon channel. The impact of some relevant parameters, namely the channel length, the interface trap density and the drain doping, on the swing factor and $I_{ON}/I_{OFF}$ ratio is discussed.

The variation of the swing factor and the $I_{ON}/I_{OFF}$ ratio in logarithmic scale versus silicon molar fraction for a channel length of 30 nm, a drain doping of $10^{19}$ $cm^{-3}$ and a drain voltage equals to 0.6 V is depicted by the plot of Fig. 2(a). This figure proves the outstanding capability of the proposed SiGe DG TFET design for making a good trade-off between both derived current capability and scalability performances. In other words, it is clearly shown from this figure that it is possible to get good values of both performance criteria for the proposed SiGe based device in comparison to the conventional Si TFET design by adopting values of the molar fraction from the set {0.15, 0.2, 0.25}, which is likely to satisfy the up to date technological constraints [23]. More precisely, taking the Ge content with 20% enables simultaneously achieving a high $I_{ON}/I_{OFF}$ ratio value of $10^8$ and a low swing factor of 35 mV/dec at the nanoscale level ($L_g = 30$ nm). Figure 2(a) illustrates also the complex subthreshold behavior of the proposed SiGe based design, where the Ge concentration induces a highly non-linear behavior of the swing factor. This phenomenon can be attributed to the quantum nature associated with the band-to-band tunneling effects, where the tunneling barrier height plays a crucial role on the TFET device performance. Moreover, it is shown from this figure that the $I_{ON}/I_{OFF}$ ratio decreases with the Ge mole fraction increase, which is mainly due to the leakage current increase as demonstrated in Fig. 2(b). This figure shows the impact of the Ge mole fraction on the drain current at ON and OFF states. It is clearly shown from this figure that the drain current increases with increasing the Ge content. The obtained electrical behavior is ascribed to the tunnel barrier lowering effect induced by increasing the Ge allowing in the SiGe channel. Moreover, the latter could also enhance the carrier mobility which could also contribute in the drain current enlargement at both ON and OFF states.




**(a)**




**(b)**

**Fig. 2** Variation of **a** both swing factor and the logarithm of ratio $I_{ON}/I_{OFF}$ **b** ON and OFF state drain currents as a function of the silicon concentration in the channel alloy (Channel length L = 30 nm, drain doping $N_d = 10^{19}$ $cm^{-3}$ and drain voltage $V_{ds} = 0.6$ V)

To physically demonstrate the effect of Ge mole fraction on the band to band tunneling mechanism, Fig. 3 depicts the band structures associated with the investigated SiGe based TFET design with different Ge mole fraction ($x = 0.1$ and $x = 0.6$) for both ON and OFF states ($V_{gs} = 0$ V and $V_{gs} = 1$ V). This figure illustrates also a zoom view for these band diagrams. It is clearly demonstrated from this figure that the minimum tunneling width of the investigated SiGe TFET design with $x = 0.1$ (W1) is about 3.8 nm, while it is W2 = 2.2 nm for the case of the Ge content of 60%. This indicates that increasing the Ge content induces the tunneling width decrease and

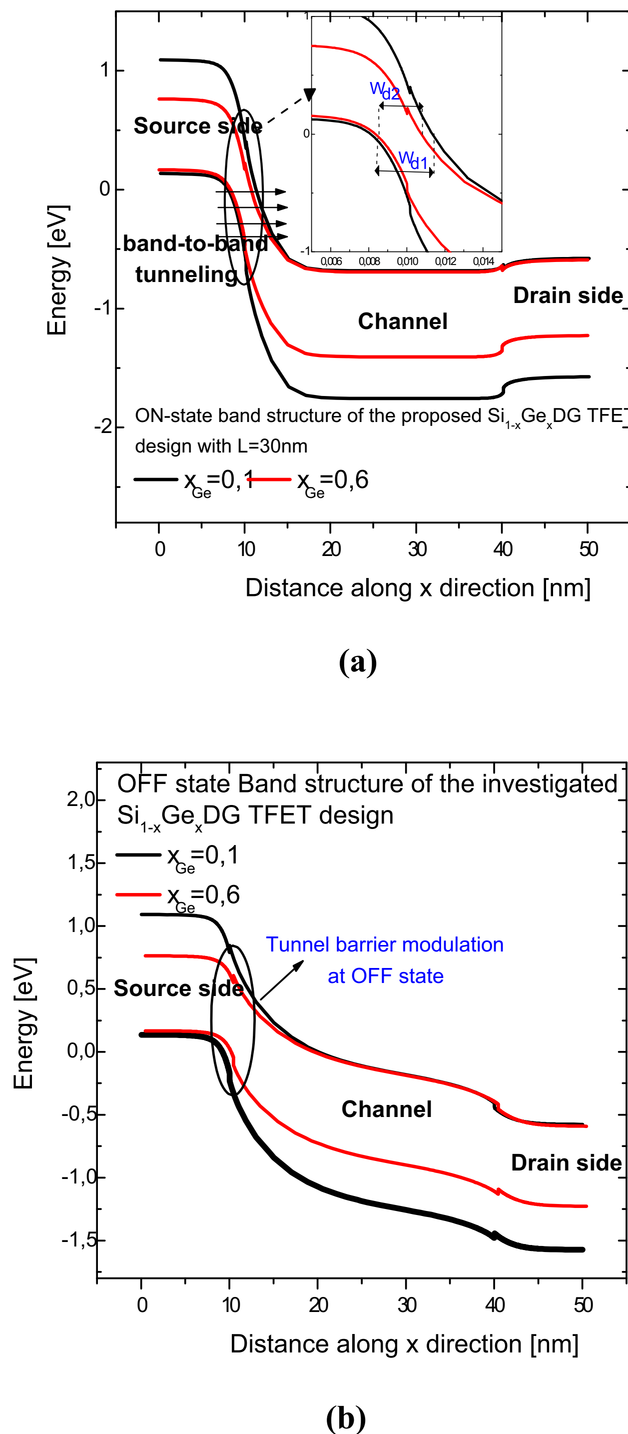
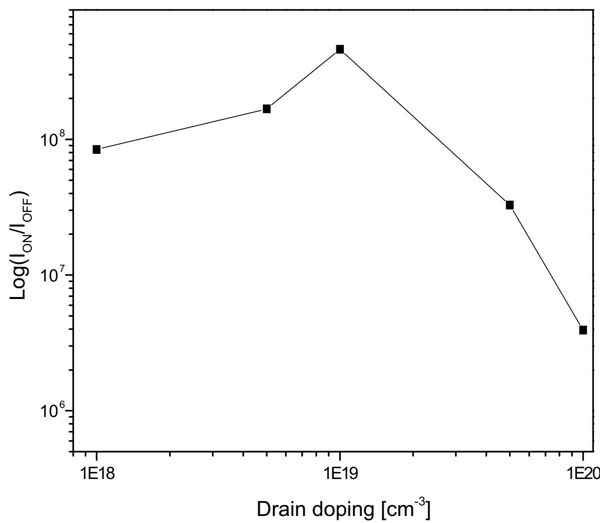



**Fig. 3** **a** ON and **b** OFF state band diagrams associated with the investigated SiGe TFET design with different Ge content (Channel length L = 30 nm, $V_{gs} = 1$ V and drain voltage $V_{ds} = 0.6$ V)

therefore opens up the route for enhancing the BTBT rate. This can, in turn, improve the tunneling current across the S/C junction for the proposed device with SiGe channel as it is shown in Fig. 2, which emphasizes the outstanding capability of the proposed SiGe TFET design for offering high electrical and switching performances.

The doping of the drain extension is of paramount importance due to its influence on the subthreshold region. In case of equal doping levels for the source and the drain extensions, the TFET device shows ambipolar behavior, which can disturb the good operation of circuits. The appropriate adjusting of the doping level at the drain side could provide the possibility for engineering the quantum tunneling barrier at the channel/drain interface enabling not only lower OFF state current but also advantageous reduction of the inherent ambipolar effect in Si-based TFET [16, 24]. However, it should be remembered that such reduction must preserve satisfactory doping to make the contact formation a feasible task [25]. Thus, the adoption of SiGe material as a channel could offer further pathways to effectively engineer the tunneling barrier and the electric field distribution at channel/drain junction, where selecting the suitable drain doping level as well as the appropriate Ge mole fraction, leading to achieve better ON to OFF current ratio seems an interesting issue and merits to be addressed. In this context, Fig. 4 illustrates the variation of the logarithm of the $I_{ON}/I_{OFF}$ ratio as a function of the drain doping concentration, which is varied from $10^{18}$ cm$^{-3}$ to $10^{20}$ cm$^{-3}$. It is found from Fig. 4(a) that the drain doping increase induces an increase on the drain current, which is ascribed to the formation of a potential barrier near the drain side. This barrier is modulated with varying the drain region doping. Basically, the channel and drain n-type doping in the TFET designs are in fact taken with different levels, where the drain side should be with high doping concentration to avoid the current degradation related to series resistance at the drain side, while, the channel doping level should be relatively low in order to unsure the BTBT mechanism at S/C interface. This drain doping difference induces a potential barrier at the interface. On the other hand, Fig. 4(a) shows that taking the drain doping around $10^{19}$ cm$^{-3}$ enables achieving a superior $I_{ON}/I_{OFF}$ ratio. This phenomenon is attributed to the complex behavior of the investigated design, where varying the drain doping level enables the modulation of potential barriers at both channel/drain and drain/metal interfaces. This can affect the drain currents at both ON and OFF states. More precisely, efficiently engineering the potential barrier at the drain/channel interface, achieved by identifying the best drain doping concentration and Ge content enables the possibility for bridging the gap between both reduced ambipolarity and high electrical performance aspects. For this reason, we consider a drain doping level equals to $10^{19}$ cm$^{-3}$ and the Ge concentration with 0.3 for the remaining simulations.

In order to explore the physical rules governing the obtained electrical behaviour associated with the impact of the drain doping concentration, Fig. 4(b) illustrates the band diagrams



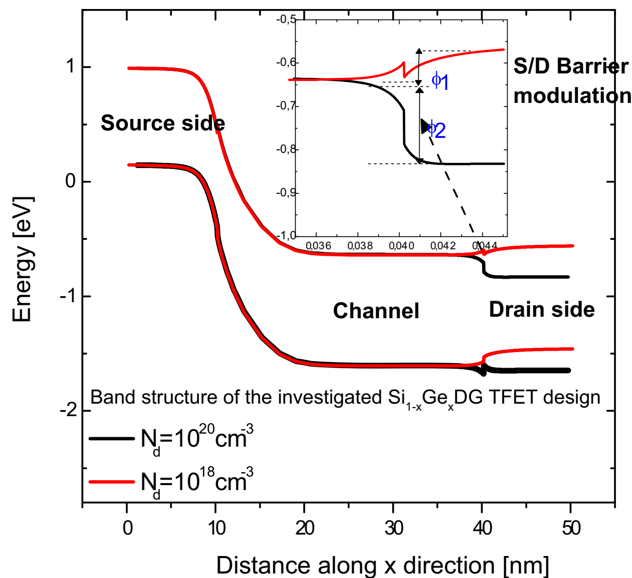




**Fig. 4** **a** Variation of the $I_{ON}/I_{OFF}$ ratio as a function of the drain doping for the SiGe TFET device (Channel length L = 50 nm, composition x = 0.3 and drain voltage $V_{ds}$ = 0.6 V). **b** Comparison of Band diagrams associated with the investigated SiGe TFET design with different drain region doping levels

of the investigated SiGe-based TFET design with dissimilar drain doping levels. Moreover, a zoom view of the channel/drain interface for these band diagrams is illustrated by this figure in which it is demonstrated that the doping difference between the channel and the drain regions induces potential barriers. It is shown that the later barrier is about 0.08 eV for the proposed SiGe TFET design with $N_d = 10^{18}$ $cm^{-3}$ while it is 0.12 eV for the case of the drain doping concentration of $10^{20}$ $cm^{-3}$ indicating the effect of the drain doping on the channel electrostatic behavior. This effect contributes in influencing the device drain current. The potential barrier at the channel/drain interface can be governed by the following equation [26].

$$\varphi_i = V_t \ln\left(\frac{N_d}{N_{ch}}\right) \tag{3}$$

where $V_t$ is the thermal voltage which is equal to 0.026 eV. This confirms that the drain doping concentration has a significant impact on the device electrical performance and can potentially modulate the channel/drain potential barrier and thereby the derived drain current capability. It is to note that the gate work-function could also influence the band structure of the investigated TFET design and can alter the potential barrier at the channel/drain interface as well as the tunnel barrier width at the source channel junction. The gate work-function is optimized in order to simultaneously ensure the cost effectiveness of the device and better BTBT capability and is fixed to 4.6 eV.

The drain current variation is highlighted in Fig. 5 as a function of the gate voltage for a drain voltage equals to 0.6 V. As indicated on this figure, the proposed SiGe device leads to a noticeable reduction in the leakage ambipolar values in comparison to the conventional device. This achievement can be explained by the effective modulation of the tunneling barrier at the channel/drain interface, where optimizing the drain doping and the Ge content can enable enormously reducing the leakage current. This results in turn into the increase of the $I_{ON}/I_{OFF}$ ratio, which offers better performance for the device in digital applications.

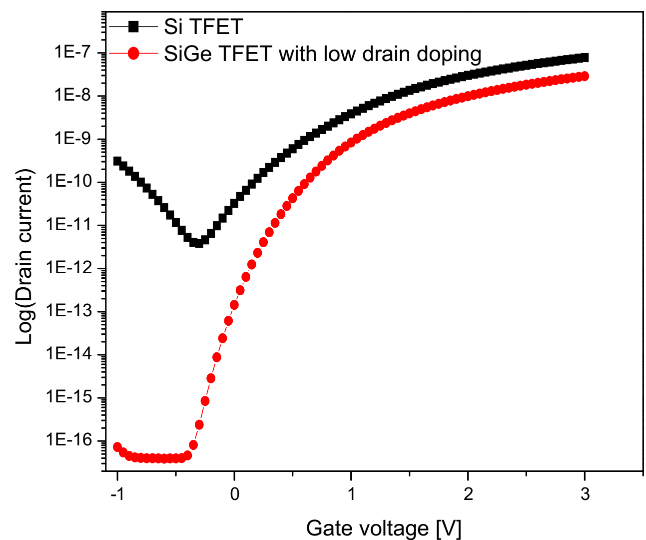



**Fig. 5** Variation of the drain current logarithm as a function of the applied gate voltage for the Si and SiGe TFET devices (Channel length L = 30 nm, composition x = 0.3, drain doping $N_d = 10^{18}$ $cm^{-3}$ and drain voltage $V_{ds}$ = 0.6 V)

In Fig. 6, the variation of the swing factor is displayed against the channel length associated with both studied devices. We observe that the swing factor decreases steadily with the channel length values for the SiGe TFET design, while the conventional Si-based device shows a faster decrease of the swing factor as a function of the channel length. Moreover, it is clearly seen that the proposed SiGe-based TFET design outperforms the conventional one, where it demonstrates lower swing factor values over a wide range of channel lengths. This improvement can be explained by the enhanced channel electrostatic behavior offered by optimizing both Ge mole fraction and drain doping level. As a matter of fact, the Ge content induces the tunnel barrier width reduction as it is confirmed by the band structures illustrated in Fig. 3, which enables enhancing the tunneling rate resulting in an enhanced subthreshold behavior as compared to the Si-based TFET structure. Furthermore, optimizing the doping of the drain current allows enhancing the derived current capability of the investigated design, where the drain doping level variation can modulate the channel/drain interface barrier as it is demonstrated in Fig. 4(b). Accordingly, the obtained results indicate the effectiveness of the proposed design for achieving improved immunity against the undesirable short channel effects.

Figure 7 reports the change of the $I_{ON}/I_{OFF}$ ratio in logarithmic scale versus the channel length. The logarithm of the $I_{ON}/I_{OFF}$ ratio is approximately unaltered by the reduction of the channel length whilst the degradation of this ratio becomes pronounced in the Si based TFET for low values of the channel length. Thus, the SiGe DG TFET device including low doped drain region exhibits better scaling capability because it is less sensitive to the degradation of performance measures when reducing the channel length.

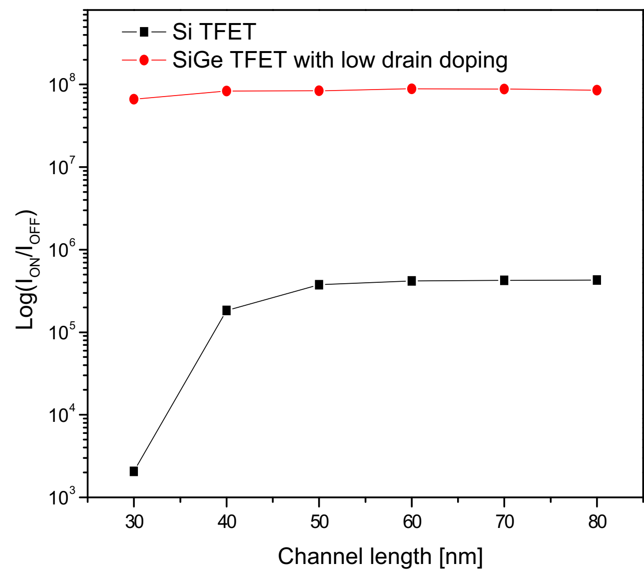



**Fig. 7** Variation of the ratio $I_{ON}/I_{OFF}$ in logarithmic scale as a function of the channel length for the Si and SiGe TFET devices ($x = 0.2$, $N_d = 10^{19}$ cm$^{-3}$ and $V_{ds} = 0.6$ V)

Hereafter, we analyze the influence of interface traps on the turn-on characteristics of both devices. In analogy to DG MOSFET structures, we assume the presence of a uniform interface trap density due to the hot carrier injection near the drain side along one third of the channel length [27]. Figure 8 introduces the evolution of the swing factor as a function of the interface traps density. It is clearly demonstrated that the swing factor of both

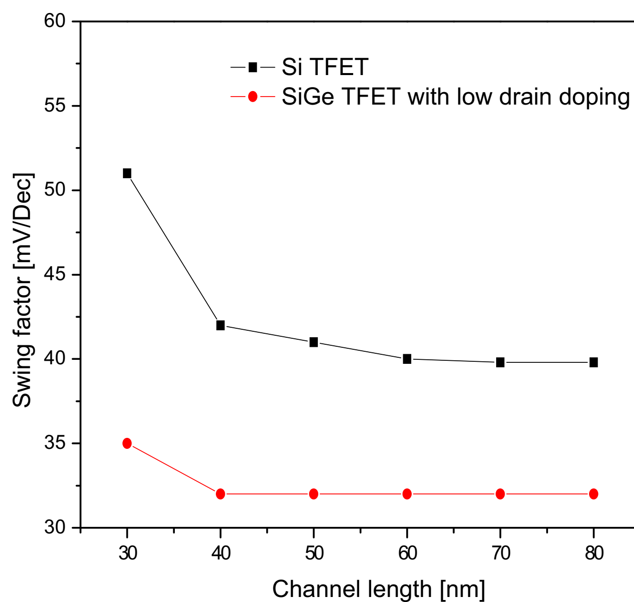



**Fig. 6** Variation of the swing factor as a function of the channel length for the Si and SiGe TFET devices (Composition $x = 0.2$, drain doping $N_d = 10^{19}$ cm$^{-3}$ and drain voltage $V_{ds} = 0.6$ V)

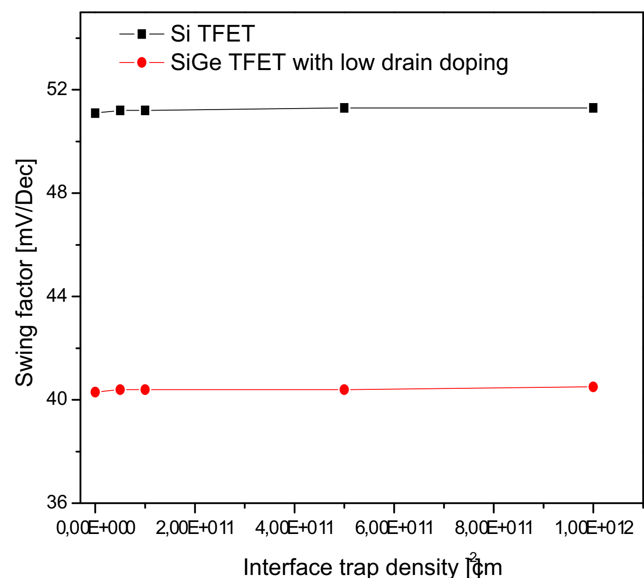



**Fig. 8** Variation of the swing factor as a function of the interface trap density for the Si and SiGe TFET devices (Channel length L = 50 nm, composition $x = 0.2$, drain doping $N_d = 10^{19}$ cm$^{-3}$ and drain voltage $V_{ds} = 0.6$ V)

devices decreases very steadily with the increase of the interface traps density.

Figure 9 reports the change of the $I_{ON}/I_{OFF}$ ratio in logarithmic scale versus the interface traps density. The logarithm of the $I_{ON}/I_{OFF}$ ratio is approximately unaltered by the presence of the interface traps whilst the degradation of this ratio becomes pronounced for the SiGe TFET for high values of the interface traps density. Ultimately, by well optimizing the Ge mole fraction and drain doping level, we were able to achieve a superior current ratio, reduced swing factor and enhanced immunity behavior. This emphasizes the effectiveness of the proposed design methodology for providing high-performance TFETs, suitable not only for digital circuits but also for analog/RF applications.

## 4 Conclusion

In this paper, we have focused on twofold objectives related to the performance of nanoscale Double Gate TFET device. First, we have investigated the scaling capability of our considered DG TFET device. Besides, we have assessed its immunity against the interface trap density located near to the drain side. The proposed design is built upon the adoption of SiGe alloy as the channel material and the reduced doping of the drain region. A comparison has been conducted with respect to the silicon based DG TFET, where a significant improvement in both the swing factor and the $I_{ON}/I_{OFF}$ ratio has been obtained.

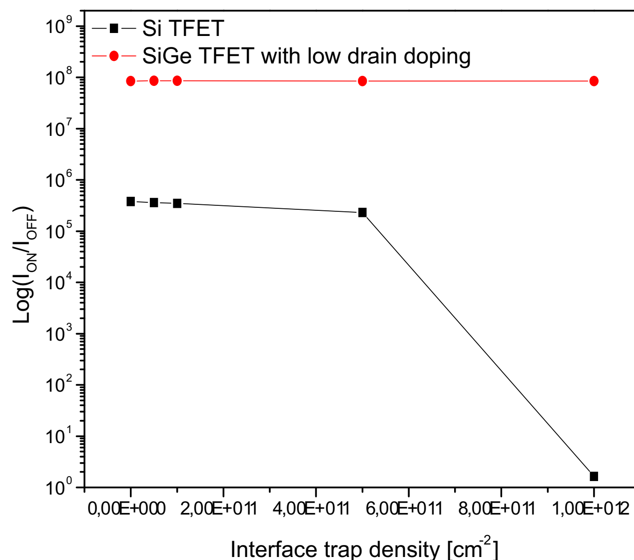



**Fig. 9** Variation of the ratio $I_{ON}/I_{OFF}$ in logarithmic scale as a function of the interface trap density for the Si and SiGe TFET devices (Channel length L = 50 nm, composition x = 0.2, drain doping $N_d = 10^{19}$ $cm^{-3}$ and drain voltage $V_{ds} = 0.6$ V)

Furthermore, it has been demonstrated based on a sensitivity analysis that the alteration of both performance measures is less pronounced in the SiGe DG TFET with respect to the variation of the channel length and the interface trap density. Hence, more efforts should be dedicated to the exploitation of the SiGe DG TFET figures of merit in the context not only of digital circuits but also analog/RF applications.

## References

1. Hu C (1991) Future CMOS scaling and reliability. Proc IEEE 81(05):682–689
2. Skotnicki T, Hutchby JA, King TJ, Wong HSP, Boeuf F (2005) The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance. IEEE Circuits Devices Mag 21(01):16–26
3. Hemmat M, Kamal M, Afzali-Kusha A, Pedram M (2017) Hybrid TFET-MOSFET circuit: a solution to design soft-error resilient ultra-low power digital circuit. Integration 57:11–19
4. Ghoggali Z, Djeffal F (2010) Analytical analysis of nanoscale fully depleted double-gate MOSFETs including the hot-carrier degradation effects. Int J Electron 97(2):119–127
5. Mamaluy D, Gao X (2015) The fundamental downscaling limit of field effect transistors. Appl Phys Lett 106:193503–193503.5
6. Djeffal F, Ferhati H, Bentrcia T (2016) Improved analog and RF performances of gate-all-around junctionless MOSFET with drain and source extensions. Superlattice Microst 90:132–140
7. Djeffal F, Lakhdar N (2013) An improved analog electrical performance of submicron dual-material gate (DM) GaAs-MESFETs using multi-objective computation. J Comput Electron 12(01):29–35
8. Tamersit K, Djeffal F (2016) Double-gate Graphene Nanoribbon field-effect transistor for DNA and gas sensing applications: simulation study and sensitivity analysis. IEEE Sensors J 16(11):4180–4191
9. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy-efficient electronic switches. Nature 479:329–337
10. Seabaugh AC, Zhang Q (2010) Low-voltage tunnel transistors for beyond CMOS logic. Proc IEEE 98(12):2095–2110
11. Esseni D, Guglielmini M, Kapidani B, Rollo T, Alioto M (2014) Tunnel FETs for ultralow voltage digital VLSI circuits: part I—device–circuit interaction and evaluation at device level. IEEE Trans Very Large Scale Integr VLSI Syst 22(12):2488–2498
12. Ferhati H, Djeffal F, Bentrcia T (2018) The role of the Ge mole fraction in improving the performance of a nanoscale junctionless tunneling FET: concept and scaling capability. Beilstein J Nanotechnol 09:1856–1862
13. Mamidala JK, Vishnoi R, Pandey P (2017) Tunnel field-effect transistors (TFET): Modelling and simulation. John Wiley, West Sussex
14. Le Royer C (2011) Interfaces and performance: what future for nanoscale Ge and SiGe based CMOS? Microelectron Eng 88(07):1541–1548
15. Mahajan R, Gautam DK (2016) Analysis of a SiGe MOSFET at 22nm. Silicon 08(04):505–511
16. Wu J, Taur Y (2016) Reduction of TFET OFF-current and subthreshold swing by lightly doped drain. IEEE Trans Electron Devices 63(08):3342–3345
17. Atlas User's Manual (2012) SILVACO TCAD
18. Seo JH, Yoon YJ, Lee S, Lee JH, Cho S, Kang IM (2015) Design and analysis of Si-based arch-shaped gate-all-around (GAA). Curr Appl Phys 15(03):208–212

19. Li ZYC, Guo J, Zhuang Y (2019) A GaAs0.5Sb0.5/In0.53Ga0.47As heterojunction Z-gate TFET with hetero-gate-dielectric. Superlattice Microst 129(05):282–293
20. Kardam U, Narang R, Saxena M, Gupta M (2019) Exploring the applicability of well optimized dielectric pocket tunnel transistor for future low power applications. Superlattice Microst 126(02):8–16
21. Tam S, Ko PK, Hu C (1984) Lucky-electron model of channel hot-electron injection in MOSFET'S. IEEE Trans Electron Devices 31(09):1116–1125
22. Abdi MA, Djeffal F, Dibi Z, Arar D (2011) A two-dimensional analytical subthreshold behavior analysis including hot-carrier effect for nanoscale gate stack gate all around (GASGAA) MOSFETs. J Comput Electron 10(1–2):179–185
23. Bentrcia T, Djeffal F, Benhaya A (2012) Continuous analytic *I*—*V* model for GS DG MOSFETs including hot-carrier degradation effects. J Semicond 33(01):014001(1–014001(6
24. Garg S, Saurabh S (2018) Suppression of ambipolar current in tunnel FETs using drain-pocket: proposal and analysis. Superlattice Microst 113(01):261–270
25. Boucart K (2010) "Simulation of double-gate silicon tunnel FETs with a high-k gate dielectric". PhD Dissertation, École Polytechnique Fédérale de Lausanne, Switzerland
26. Chebaki E, Djeffal F, Ferhati H, Bentrcia T (2016) Improved analog/RF performance of double gate junctionless MOSFET using both gate material engineering and drain/source extensions. Superlattice Microst 92:80–91
27. Bentrcia T, Djeffal F, Chahdi M (2013) An analytical two dimensional subthreshold behavior model to study the nanoscale GCGS DG Si MOSFET including interfacial trap effects. Microelectron Reliab 53(04):520–527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