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Development of new multilevel power converter structure for grid-connected renewable energy systems

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Presented by:

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I dedicate this work to:
Djamal, Wassila My parents
Imane, Meriem, Aya, Ritege and Soheib my siblings
Aida, Hada and Abderahmane, Amar My grand parents
My thesis director BARRA Kamel
Everyone who helped me even with a nice word

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ملخـــــــــــــــــص

تَقْتَرِحُ هاتهِ الأطروحةُ مُساهمتَيْنِ رئيسيّينِ، تَتمثل الأولَى في عاكسٍ مُحسّنٍ مُتعددِ المستويات سُمي هذا العاكس بـ : العاكسُ WT-type وهو مشتقٌّ من عاكسٍ تقليدي، أمَّا الثانِيةُ فَتَتمثل في خوارزميةِ تحكُمٍ مُقترحةٍ قائمةٍ على تقنيةِ التحكم FS-MPC والتي تقوم بمنعِ انقطاعِ اشتغالِ أنظمةِ توليدِ الطاقةِ في حال حدوث عطبٍ في العاكس. دفع انخفاض تكلفة الطاقة المتجددة العديد من البلدان إلى بدء استغلال مصادرها المتجددة، لا سيما تِلك التِي تملكُ إمكاناتٍ عاليةٍ، على سبيل المثال : الجزائر. يُمكن لموقع صغير جنوبَ هذا البلد أن يُلبّيَ حاجةَ العالم بأسرهِ منَ الكهرباء، لذلك قمنا بعرضِ العديدِ من المشاريع التي تم انشاؤها كمحاولةٍ للتقليل من الاعتماد على النفط. نظرًا لأن محطاتِ الطاقةِ الشمْسيّةِ يمكن أن تأخذ أشكالا و هَياكلَ مختلفةً تَطوَّرتْ بِمرور الزَّمنِ، نَستعرضُ هياكِلَهَا المختلفةِ وبعض المفاهيم الأساسية حول الطاقة المتجددة و التي تساعدنا في فهم وتقييم أنظمةَ هَاتهِ الطاقةِ. أيضًا، نَعرِضُ دراسةً لِنظامِ شمسيٍّ (PV) بإستطاعةِ 3 كيلو وات يتم التحكم فيه باستخدام تقنية نموذج التحكم التنبئي من نوعِ المجموعات المُتنهية (FS-MPC) في حالته العادية، و أيضًا في حالة وقوع عطب مّا في العاكس. في هذا الصددِ، نَقترحُ تقنيةً مرتكزة على نموذجِ التحكم التنبئي من نوعِ المجموعات المُتنهية FS-MPC للتعامل مع سيناريوهين مُحتَمليْنِ للعطبِ : عطبٌ من نوع الدارة المُستَقْصَرةِ في مكثفِ وَصْلَةِ التيارِ المُستمرِّ الخاصّ بالمدخلِ، أما الثاني فيتمثل في عَطَبِ الدارّةِ المفتوحةِ للـ IGBT .أيضًا بعْدَ عرضٍ موجزٍ للإنتاج البَحثيّ لِلعاكسات مُتَعددة المستوى في الأبحاثِ المُحَكَّمَةِ، نقارن نتائج مُحاكاتِها الحاسوبيّةَ مِن حيثُ جودةِ تيّارِ الحمولة و تشوهه THD . أخيرًا و ليسَ آخرًا، قَدَّمنَا مُراجعة مُستفِيضَةً لأنواع عاكسات من نوع T و تم ترتّيبُها على سُلّم زمني وفقا لسنة إصدارها. بعد ذلك ، يتم معاينة خصائص العاكس المقترح بشكل معمق. ثم يتمّ وضع هذا العاكس تحت الإختبار للتحقق من ميزاته. آخِرًا، نعرض نتائج العمل المخبري ونقوم بمناقشة هاته النتائج و التي تم الحصول عليها بفضل استعمال متحكم من نوع Dspace 1104 .

الكلمـــات المفتاحية :

التتبع الأعظمي للطاقة، نموذج التحكم التنبئي من نوعِ المجموعات المُتنهية ، التحكم في الانظمة الشمسية في حالة عطب ، عاكس متعدد المستويات ، عاكس جديد متعدد المستويات ،عاكس WT ، نظام الشمسي المتصل بالشبكة ، مراجعة للعاكسات متعددة المستويات.

Abstract

This dissertation presents two main contributions, an optimized multilevel inverter called WT-type inverter which is derived from the classical T-type inverter, and a proposed control algorithm based on FS-MPC technique that prevents the interruption of power generation systems in case of a failure of the inverter. The falling cost of renewable energy (RE) encouraged lot of countries to start exploiting their renewable sources, particularly those with a high-potential for example: Algeria. A small site in this country can respond to the world's demand for electricity, thus we present the several projects installed to reduce dependency on oil. As photovoltaic plants can take different forms and structures which developed over time, we walked through it various structure and some basic concepts about RE which help understand and assess these power systems. We exhibited the study of a 3kW photovoltaic system controlled using Finite-set Model predictive Control (FS-MPC) in regular and faulty operation. An FS-MPC-based technique is proposed to tolerate two fault scenarios: a short-circuit in a dc-link capacitor, and an open circuit breakdown of an IGBT. After a brief overview of multilevel inverters, simulation results are compared in terms of the quality of the load current. Finally, we presented an extensive review of T-types base multilevel inverters and organized them according to their year of issuance on a timescale. In addition, a new inverter circuit WT-type is presented with its detailed procedure of optimization from the classical T-type inverter. Then, this inverter is put for examination of its features, a practical validation was carried out using the Dspace 1104 control card and the obtained results were discussed and interpreted.

Keywords: Maximum Power Point Tracking mppt, MPC, finite set model predictive control, FS-MPC, Fault tolerant control, optimized multilevel inverter, novel multilevel inverterWT-type, grid-connected PV system, nine-level multilevel inverter, T-type review, T-type survey.

Résumé

Cette thèse présente deux contributions principales, un onduleur multiniveau optimisé appelé onduleur de type WT qui est dérivé de l'onduleur classique de type T, et un algorithme de contrôle proposé basé sur la technique FS-MPC qui empêche l'interruption des systèmes de production d'énergie en cas de défaillance de l'onduleur. Le coût décroissant de l'énergie renouvelable a encouragé de nombreux pays à commencer à exploiter leurs sources renouvelables, en particulier ceux ayant un potentiel élevé, comme l'Algérie par exemple. Un petit site dans le sud de ce pays pourrait répondre à la demande mondiale d'électricité. C'est pourquoi nous présentons plusieurs projets qui ont été mis en place pour tenter de réduire la dépendance au pétrole. Étant donné que les centrales solaires photovoltaïques peuvent prendre différentes formes et structures qui ont évolué au fil du temps, nous passons en revue leurs différentes structures ainsi que quelques concepts de base sur l'énergie renouvelable qui nous aident à comprendre et à évaluer ces systèmes énergétiques. Nous présentons également une étude sur un système photovoltaïque de 3 kW contrôlé par la technique de commande prédictive par modèle à ensemble fini (FS-MPC) en fonctionnement normal et en cas de défaillance de l'onduleur. Dans ce cadre, nous proposons une technique basée sur FS-MPC pour faire face à deux scénarios de défaillance potentiels : un court-circuit dans le condensateur du bus continu d'entrée et un circuit ouvert de l'IGBT. Après une brève présentation des travaux de recherche sur les onduleurs multiniveaux dans la littérature, nous comparons les résultats des simulations en termes de qualité du courant de charge et de distorsion harmonique totale (THD). Nous présentons une revue approfondie des différents types d'onduleurs de type T, classés sur une échelle de temps selon leur année de publication. Ensuite, les caractéristiques de l'onduleur proposé sont examinées en détail. Cet onduleur est alors mis à l'épreuve pour vérifier ses avantages. Enfin, nous présentons les résultats expérimentaux obtenus grâce à l'utilisation du contrôleur Dspace 1104, et discutons de ces résultats.

Mots clés : Point de Puissance Maximale, mppt, contrôle prédictif du modèle, MPC, contrôle prédictif du modèle à états fini, FS-MPC, Contrôle tolérants aux pannes, onduleur multiniveau optimisé, nouvelle topologie, onduleur multiniveau type WT, système photovoltaïque connecté au réseau, onduleur multiniveau à neuf niveaux, état de l'art des onduleur en type T

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General introduction

Overview

After the oil crisis in 1973 and the nuclear incidents of Chornobyl in 1986, the interest in an alternative, environment-friendly source of energy was at its peak, and governments started to increase investments in research in this field. Since then, several types of safe renewable energy emerged and matured for example: solar energy, wind energy, geothermal energy, biomass energy and hydropower. Nevertheless, the dynamic of integration of these energies in the principal grids is relatively slow. With the unprecedented greenhouse emissions (CO_2, CH_4 ...) and after the Russian-Ukrainian conflict, the international community were oriented to large-scale integration of these safe renewable energies.

Renewable energy is a multidisciplinary field, it gathers many specialise under one umbrella, for instance: **mechanical engineering** which deals with the moving parts such as the blades of wind turbine and hydropower turbines, **physics and chemical Engineering** which focus on bioenergy production such as the conversion of biomass into biofuels, biogas, developing photovoltaic (PV) panels on the molucular scale to improve their efficiency, **geology and geophysics** which is relevant to geothermal energy exploration, drilling and heat sources, **civil engineering** which is responsible for site assessment, foundation and structure design of renewable energy installations, such as hydropower dams wind turbines, **cyber security** which emerged with smart grids to protect safe communication between the control and the power circuit, and also protecting real-time energy production data from unauthorized access [1], and last but not least **electrical engineering** which studies the flow of energy from the source to load in addition to the hardware devices responsible for that. This field covers the whole generation process starting from the source of energy (PV, wind,..), then ensuring an optimal extraction of the energy by proper operation of the dc-dc converter and the dc-ac converter, to finally reach the grid [2].

Research problem

Large-scale integrated photovoltaic systems can be designed in various structures. These structures were gradually evolving over time in order to give a better quality of integrated energy and maximum yield, for instance: *centralised power plants* where all plants are interfaced with the grid through one DC-AC inverter. This later was developed to the *string structure* which connects an inverter to each string of PV panels. Researchers established a better structure called *multi-string structure* which introduces dc-dc choppers for each string to extract the maximum power then these choppers are connected to the grid through one common DC-AC inverter [3].

In the DC-AC part, a two-level voltage source inverter (2L-VSI) is the topology widely used in the industry. However, this inverter suffers from a bad output power quality not to mention that it is not able to operate in high voltage operation. To cope with these drawbacks, researchers proposed categories of multilevel inverters which deliver satisfying output power quality ensuring a staircase output voltage wave and offering the possibility to operate in medium and relatively high voltage ranges (6KV-7KV). Nonetheless, these multilevel inverters have a cumbersome power circuit with a complex control circuit due to the large number of components with passive elements such as capacitors which made it costly and impractical.

For large and medium power generation scales, plants are usually located in hard environmental conditions and remote places. Thus various components of the system are exposed to wear-out and failures. Despite inverters present only 10%-20% of the initial cost of the system, they could be replaced from 3 to 5 times during lifetime of the insallation as shown in Figure 0.1 [4]. Furthermore, industrial statistics have shown that PV inverters are the cause of 37% of the unscheduled maintenance and 59% of the additional repairing cost [5].

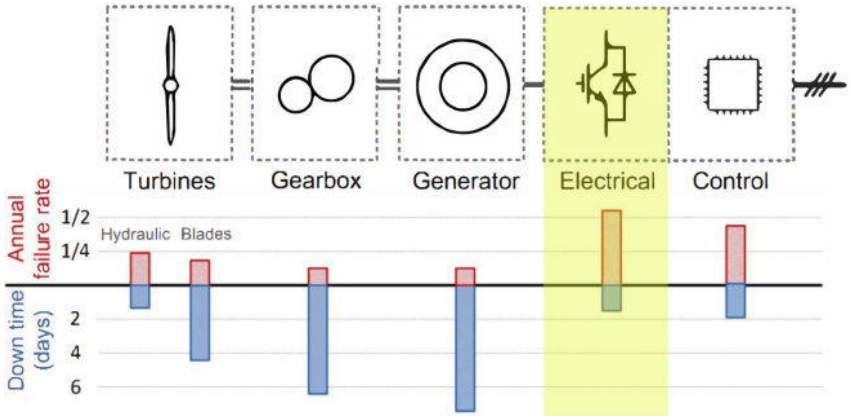

Figure 0.1 – Distribution of failure occurrence among the different parts of a wind system. [4]

In light of the problems stated above, this work will endeavour to answer the following questions:

Problem 01: Is it possible to optimise one of the existing multilevel inverters in order to offer a novel inverter topology with fewer components, and better cost-efficiency feature that can be easily implemented at high levels with a less complex control?

Resolving strategy: *A good start is to make an extensive literature review about all the multilevel inverter topologies proposed by researchers. After that, it is primordial to analyse all the converters by noticing the differences between their mathematical models. Building control designs for various topologies will offer broad flexibility to correctly design the control of a potential new inverter. A simulation and comparison between their performances would be a great metric to well understand their operation. With that being done, some inverters will stand out as good candidates for optimisation.*

Problem 02: The main goal of power plants is to produce and sell electricity. With the inevitable breaking down of inverters as shown in figure 0.1 and thus the inevitable stopping of power generation and loss of benefits, is there a way that ensure the continuity of the service until full restoration of the regular operation?

Resolving strategy: *The stopping of the system requires time to repair the failure which is undesirable. smart control would be able to ensure the continuity of the service without interruption. This means that we can still be driving the inverter by segregating the breaking parts and working with the rest healthy components. This could be possible for instance by controlling the inverter to produce 7-levels instead of 9-levels.*

All these questions are grouped under the title of the thesis: "Development of new static multilevel inverter structures for grid-connected renewable energy systems"

Research Motivations

As the title of the dissertation indicates, the aim of this work is to develop and propose a multilevel circuit that is derived from the classical T-type inverter as detailed in Chapter 4. This inverter is designed to achieve a remarkably lower overall cost and also a better efficiency compared to the classical topologies. The study aims to reduce the number of multilevel inverter IGBTs and hence becomes more cost-efficient, especially at higher levels. Also, the design procedure of the inverter takes into consideration offering

more degrees of freedom in choosing the inverter characteristics. Also, manufacturing limitations are overcome by introducing ultrafast diodes that have much better performance than the body diodes integrated into IGBTs of the classical inverter.

To solve the high rate of breaking down of controllable switches in renewable systems, and the on-site engineer's replacement which could be dangerous and costly, Chapter 2 introduces a second contribution and presents in detail a proposed control method in case of failure operation. It prevents the interruption of power production and guarantees a power quality generation that matches the IEEE standard without intervention on the power circuit level, or introducing additional components. This control technique is examined for 2 scenarios of failure. This technique is applied to a 9-level T-type inverter.

Chapters outline

In **chapter 1**, we start by taking a glimpse on the types of promising renewable energy sources that have great potential to be among the principal sources in the near future. Algeria enjoys a wide solar potential which is able to fulfil the world's demand for electricity [6]. Thus, we run through an overview of the situation of PV energy in our country, as well as the projects launched to fortify the share of renewable energy against fossil-based production in the country. After that, we talk about PV systems, their structures with their development over time. In addition to that, we explain basic knowledge about PV energy generation and introduce concepts that help understand and assess renewable power plants.

Chapter 2 starts with an introduction about the different parts that constitute a PV system. PV systems are generally composed of DC-DC converters cascaded with DC-AC inverters connected to the load/grid. Each of the previous parts is extensively explained in this chapter. The chapter is divided into two parts, the first one deals with the healthy normal operation of a 3kW PV system displaying the simulation results. The second part talks about the various types of failures that occur in PV systems and treats different failure scenarios. The proposed control technique is then implemented to reject and redeem the safe operation of the system, and the results of the system before and after the failure are compared according to various criteria.

Chapter 3 walks through a state-of-the-art of various multilevel inverter topologies proposed in the literature and their control techniques. The introduction talks about the limitations of classical inverters 2L-VSI that led to the invention of multilevel inverters. This later succeeded in using the same components of a 2L-VSI to operate at higher

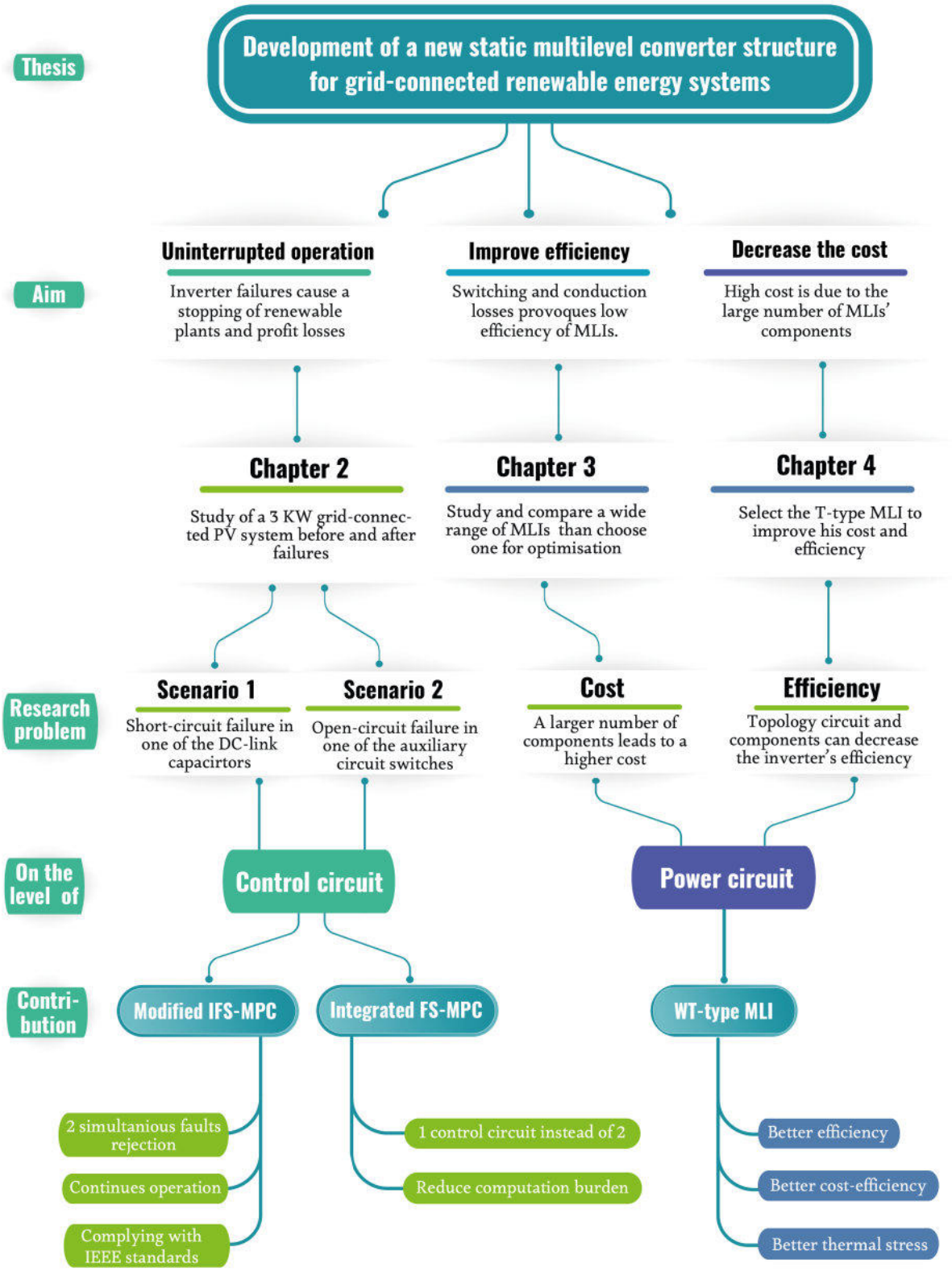

Figure 0.2 – Flowchart of the research strategy of the thesis.

voltage ranges. However, classic multilevel inverters were struggling with multiple problems like the complexity of their control and capacitors' balancing, not to mention the inability to practically go higher in levels. The pros and cons of the classic multilevel inverters in addition to multiple emerged topologies are explained where each inverter is analysed individually. The second section of this chapter tackles the control techniques of multilevel inverters which underwent a remarkable developement over time where a lot of techniques have emerged. The last section of this chapter shows the simulation results of the aforementioned multilevel inverters using Model Predictive Control.

Chapter 4 starts with a comprehensive review of T-type-based multilevel inverters by showing the two forms of the standard (classical) T-type inverter. After that, each T-type-based multilevel inverter proposed in the literature is analysed individually. All the covered multilevel inverters are organised on a timescale from 2014 to 2023. Then comes section two, where we introduce a systematic procedure for optimisation of the classic T-type inverter, with illustrations attributed to each step. This optimisation results in a proposed converter called wings T-type multilevel inverter (WT-type multilevel inverter). In part three, the intrinsic features of this converter are revealed and assessed according to various criteria such as number of components, cost, thermal stress, losses and freedom of selecting characteristics. Using the model of the converter, the Finite Set Predictive Control (FS-MPC) technique is used to drive the studied inverter. We realized the PCB board of the proposed new topology WT-type multilevel inverter based on IGBTs (FGH 60N20) in the LGEA laboratory. The WT-type multilevel inverter was underwent under several conditions and different loads to examine its performance using DSpace board 1104. Finally, The results of practical validation are interpreted and discussed.

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Chapter 1

Renewable energies and photovoltaic systems overview

1.1 Renewable energy sources

Fossil fuels are the primary source of energy in the world thanks to the high power they can produce. Despite that, these energy sources cause severe consequences on many ecosystems in addition to their emission of greenhouse gases. Operating power plants alone present approximately 35% of global greenhouse gases emitted to the atmosphere. [1]

Around the world, almost 80% of the population lives in countries that are dependent on fossil fuels. Therefore, approximately 6 billion people are exposed to crises and shocks in case of a shortage of this energy source. Meanwhile, renewable energies are available in all nations. By 2050, 90% of the world's energy can come from renewable sources as forecasts the International Renewable Energy Agency (IRENA). [2] [1]

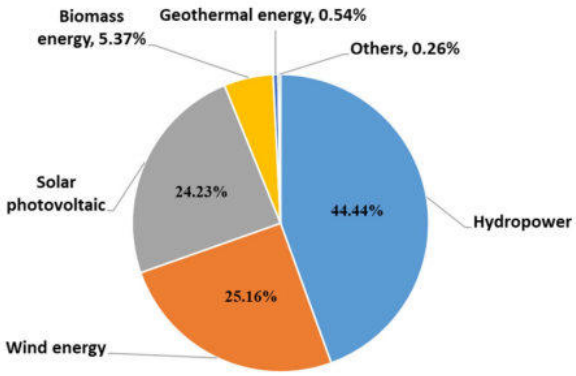


Figure 1.1 – The proportional contribution of various renewable energy sources to electricity production, Figure source: [3]

1.2 Types of renewable energy systems

Renewable energy is the energy generated from natural resources to neutralize carbon emissions and limit greenhouse gases. In 2018 the global share of renewable energy is around 14% and is expected to increase to 90% in 2050. Figure 1.1 shows the share of various types of renewable sources in the global clean production of electricity.

Renewable energy sources can be evaluated using several factors: their sustainability, technical characteristics, such as integration with other resources, energy efficiency, and operating costs [4]. These factors are important as they assist policymakers in selecting a suitable renewable energy source that meets the market demand and defining the suitable renewable energy resource to exploit.

Figure 1.2 depicts the types of renewable energy systems treated in the literature in accordance with their source of energy [5]:

(i) solar energy, which is generated from sunlight. This category is one of the most rapidly growing categories among the various types of global energy production. Solar energy includes solar photovoltaic grid-connected, solar photovoltaic standalone, and thermal solar energy [6].

(ii) Wind energy is the generation of electricity for residential and industrial use by the utilization of wind power. Wind power is converted to electricity with the help of a wind turbine. Wind energy generation can be used as a small-scale system, which supplies for instance limited regions, or as a grid-connected system, which is usually constructed in giant wind farms [7]. Wind and solar power systems are weather-dependent energies. Therefore, it is primordial to make a viability study and to take into consideration weather changes to select the most suitable site.

(iii) Geothermal energy is extracted from the earth's heat or from the steam emitted from the hot layers under the ground. Geothermal energy is able to provide industrial-scale electricity [8].

(iv) Biomass energy is extracted from organic sources like plants and animals' waste. This energy is produced by the combustion of wood, agricultural residues, and animal waste. Biomass can generate not only electricity but also heat. Besides, it can provide biofuel and biogas using anaerobic digestion, or pyrolysis/ hydrothermal carbonization, therefore, the Energy derived from waste like animal, human, or vegetable sources is considered as a subset of biomass energy [9] [10].

(v) Hydropower is obtained by converting the kinetic energy of water usually in dams or rivers into electricity. Water at a high altitude is followed by hydro-turbine to generate electricity. This renewable source is considered the largest renewable energy source in terms of the amount of generated power with a generation capacity of approximately

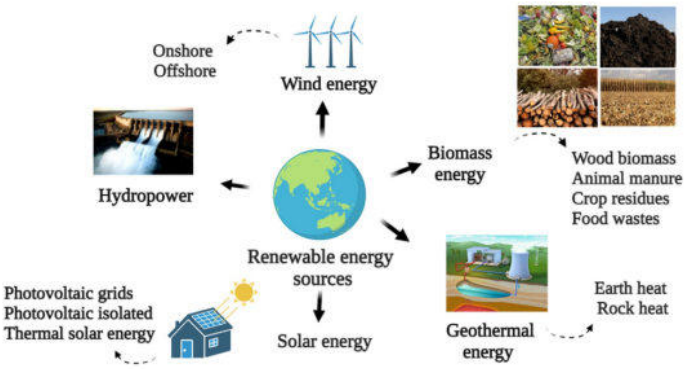


Figure 1.2 – Categories of renewable energy systems reported in the literature

1150 GW on a global scale. [11] [12].

1.3 Cost of renewable energies

In most of the world countries, renewable energy will soon be the cheapest source of energy. During only one decade, the costs of renewable energy power generation have dramatically decreased. As shown in Figure 1.3 between the years 2010 and 2019, the cost of solar energy greatly decreased by 88%. Meanwhile, the costs of onshore and offshore wind energy fell by 68% and 60%, respectively. It is expected that by 2030, renewable energy sources will be able to provide 65% of the world's electricity supply. Furthermore, they will be able to neutralize 90% of the carbon emissions from the electricity industry by 2050. The additional renewable energy generation capacity declared in 2021 was 257 GW, which is 41% higher than the 182 GW added in 2019 [2].

1.4 Renewable energy in Algeria

Algeria is noteworthy for its outstanding features, location, wealth, gas and oil reserves, size, and renewable energy potential. In addition to that, it enjoys over 3,000 hours of sunlight annually, which gives it considerable solar potential. However, it ranks 3rd in the African continent in terms of carbon dioxide emissions (CO_2) [14].

Currently, Algeria generates a small amount of its electricity from renewable sources, that is 686 MW (3%) of the total power generation annually, shared among wind (10 MW), hydro (228 MW) [15], and solar (448 MW).

Hydrocarbon resources support an overwhelming part of the Algerian economy. By 2035, Analysts predict that Algeria will need to forego hydrocarbon export revenues to supply local power demand if it won't enrich its power generation mix with important

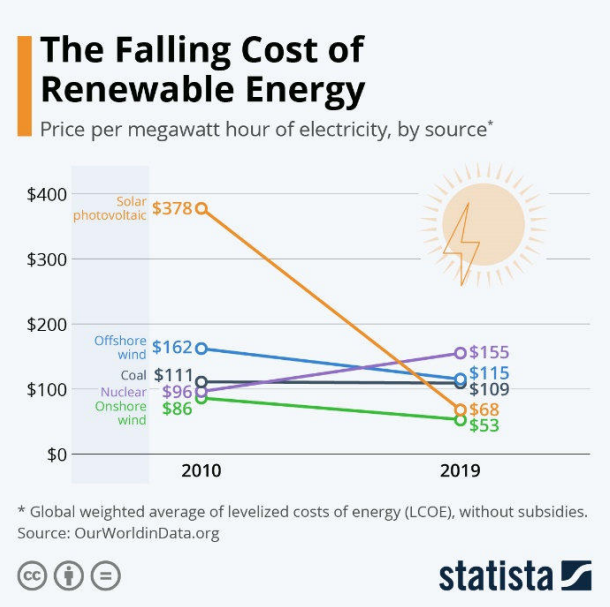


Figure 1.3 – The decreasing cost of renewable energy, source: [13]

renewable resources. Therefore, it is high time for the country to reconsider working on its renewable energy capabilities.

Algeria's most abundant renewable resources are solar, wind, hydro, and biomass. Regarding solar power potential, the country is home to some of the highest solar irradiance levels in the world, with the capacity to generate from 1,850 to 2,100 KWh/year in its desert. For wind, Algeria enjoys a 1,300 km Mediterranean coastline with wind speeds of around 8 m/s, not to mention the winds coming off the region of the Sahel in the South.

1.5 Photovoltaic power generation in Algeria

Algeria plans to produce 27% of its electric power from renewable resources mostly solar power by 2035 in multiple solar deposit sites as shown in Figure1.4. In order to boost the country's energy transition, in 2021, the Algerian government signed new agreements and partnerships in renewable energies with multiple countries: China, the United States, and Germany. These cooperations aim to forge relationships with foreign engineering services, storage systems, and solar application kits for agriculture. In the middle of this race, unfortunately, the contribution of the local universities and research centres is limited if not absent despite the huge engineering capabilities available in the country [16].

In this context, in 2021 Algeria launched a tender for a 1 GW solar energy project distributed on 5 sites ranging from 50 to 300 MW for each one. Algeria's national oil company Sonatrach, is launching considerable solar power projects for some of its off-

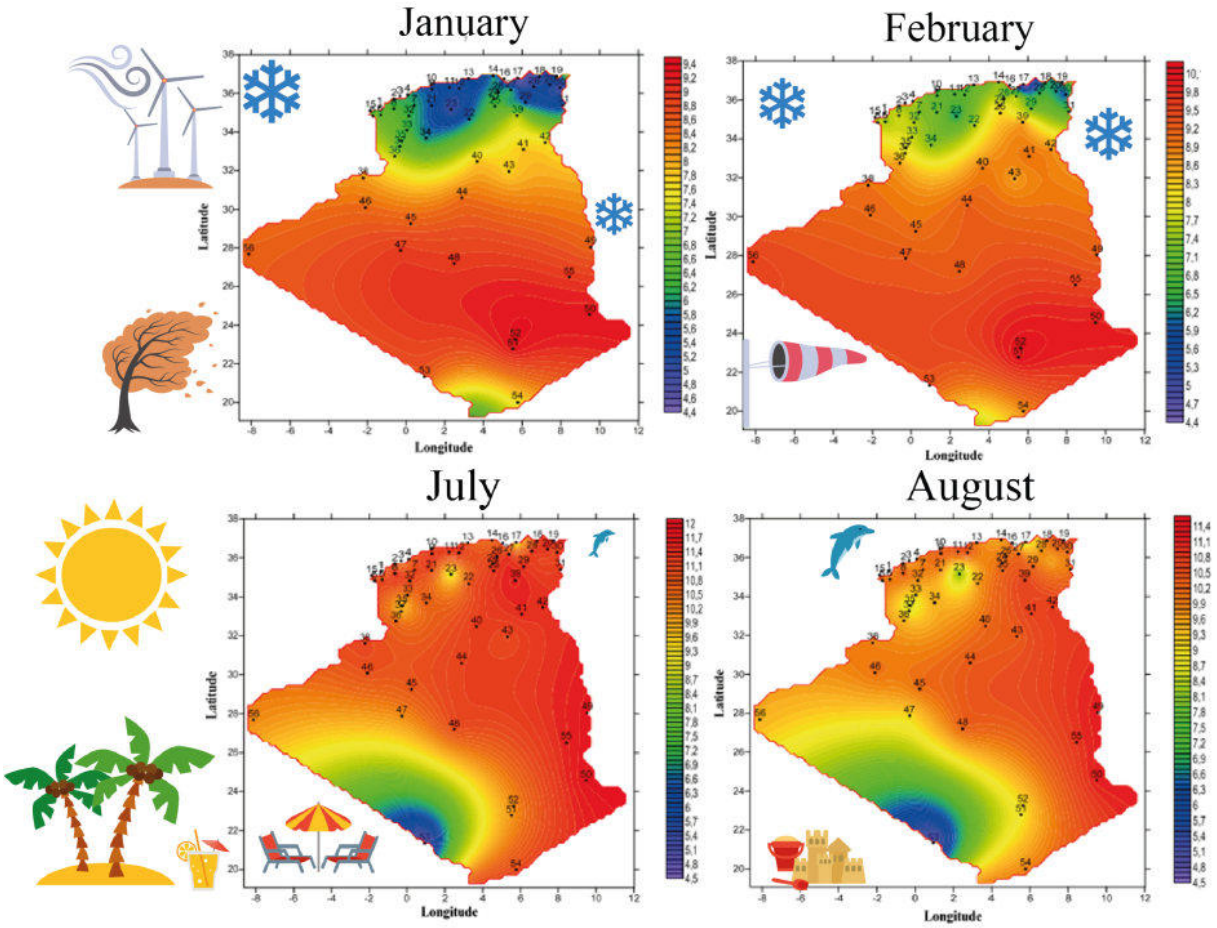


Figure 1.4 – The monthly average irradiation in winter (Jan-Feb) and summer(Jul-Aug), in Algeria [17].

grid oil/gas facilities. Sonatrach and Sonelgaz created SHAEMS company specialized in the field of renewable energy projects to deal with companies pursuing renewable energy projects. Companies from Egypt, the UK, Germany, Italy, China, and Spain are already working on renewable energy projects in Algeria.

1.5.1 Sonelgaz Algeria Solar PV Park (2015, Adrar)

This Sonelgaz project is located in Adrar. It is a Solar PV Park with a capacity of **233MW**. The project was constructed and completed in 2015 and was developed by China Hydropower Engineering Consulting Group; Yingli Green Energy, Sinohydro, Shariket Kahraba oua Takat Moutadjadida.

1.5.2 Ouargla Solar PV Park (2015, Ouargla)

This project is located in the wilaya of Ouargla. It is a **30MW** Solar PV Park project which came into service in 2015. The project was constructed by China Hydropower Engineering Consulting Group; Sinohydro; Yingli Green Energy and Shariket Kahraba oua Takat Moutadjadida.

1.5.3 Laghouat Solar PV Park (2016, Laghouat)

A **60MW** solar PV power project is located in Laghouat, southern Algeria. It was developed in 2016 by China Hydropower Engineering Consulting Group; Sinohydro; Yingli Green Energy and Shariket Kahraba oua Takat Moutadjadida which owns the project.

1.5.4 Djelfa Solar PV Park (2016, Djelfa)

In Djelfa 500 km south of the capital Algiers, a Solar PV Park of a **53MW** project was set up and commissioned in 2016 by China Hydropower Engineering Consulting Group; Shariket Kahraba oua Takat Moutadjadida which is the owner of the project; Sinohydro; Yingli Green Energy.

1.5.5 Hauts Plateaux West Saida Solar PV Park (2016, Saida)

In the wilaya of Saida, The Hauts Plateaux **30MW** Solar PV Park project is located. It has been operating since 2016. The project has been commissioned by Shariket Kahraba Oua Takat Moutadjadida.

1.6 Photovoltaic systems

1.6.1 Introduction

The term *'Photovoltaic'*, usually abbreviated as PV, is made up of two words: the Greek word *'phōtós'*, which means the light, and the family name of the physicist *Alessandro Volta*. The most basic component that converts the sun's light into electricity is the solar cell. Basically, solar cells are fabricated from the semiconductor material silicon. They deliver voltages of approximately 0.5V, and a current varies between 0 and 10A depending on the cell and radiation. To achieve usable voltages and currents, solar cells are connected in series and are gathered in a "module" in which they are protected against environmental factors like moisture and mechanical damage.

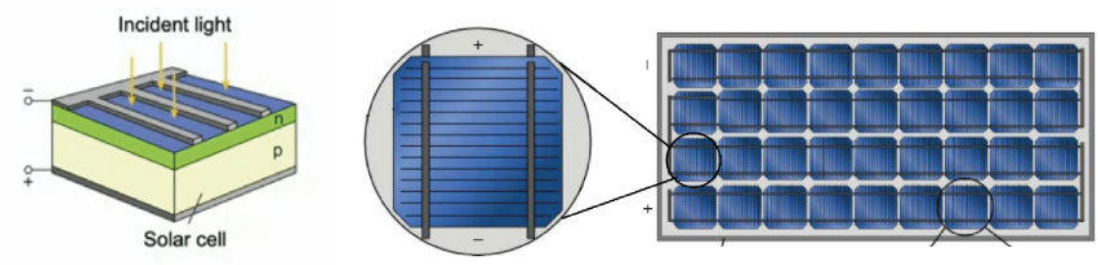
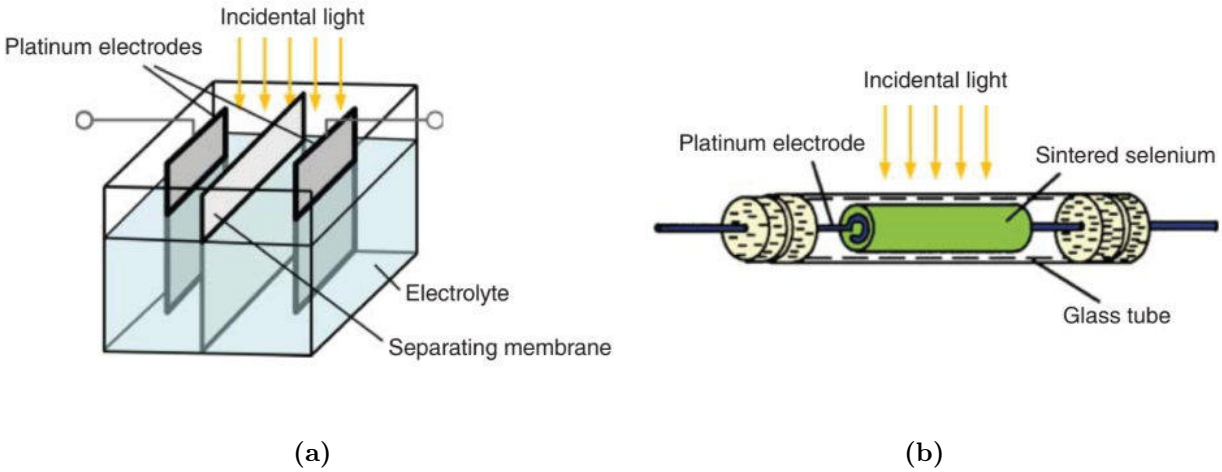


Figure 1.5 – Shows the composition of a typical silicon cell.

1.6.2 Brief history on PV systems

In 1839, the scientist *Alexandre Edmond Becquerel* discovered the photoelectric effect while conducting electrochemical experiments. He placed two platinum electrodes in an electrolyte and measured the current flowing between the two electrodes as shown in Figure1.6a. He noticed that the intensity of the current varies when exposed to light. it was a matter of a photo-effect.



(a) **(b)**

Figure 1.6 – Shows (a) Electrochemical experiment of Becquerel (b) the first ever solar cell by Adams.

In 1876, William Adams and Richard Day found out that a selenium platinum rod electrode like in Figure1.6b can generate electricity when it is exposed to light. By this, it was proved that a solid body can directly convert light energy into electrical energy. This is how the first ever solid-state solar cell was built.
The first module was then produced with an area of approximately 30 cm^2 with an efficiency of almost 1%. In 1954, the first ever silicon solar cell was fabricated with an area of 2 cm^2 and an efficiency of 6 %. The first industrial application was in 1958 when the satellite Vanguard 1 was launched into space equipped with six silicon solar cells attached to its surface. For 6 years, the satellite was operated using those small silicon solar cells.

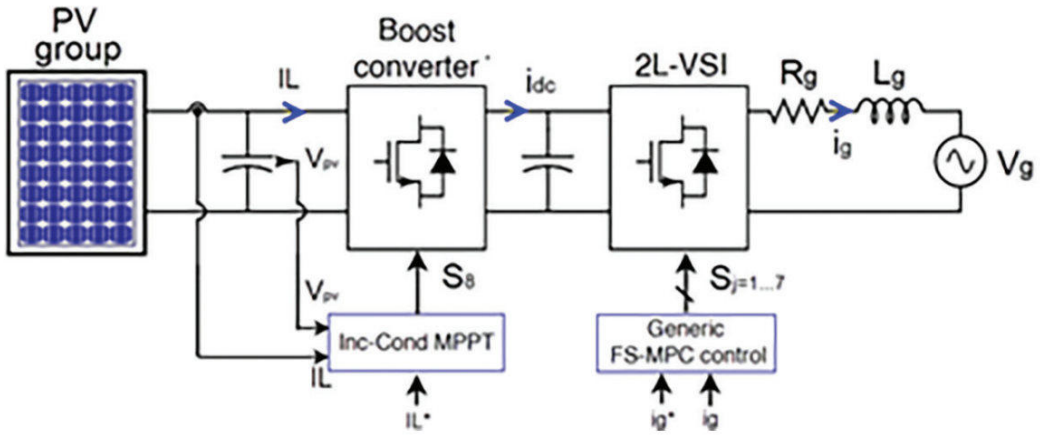


Figure 1.7 – General PV system scheme controlled using separated control circuits.

1.6.3 Power converters in PV systems

In a PV system, we frequently find two types of power converters: choppers and inverters. These converters contain a power circuit part and a control circuit. The aim of DC-DC converters is to convert the DC voltage to another voltage level by mean value variation, which is done with the help of the control circuit. This later can assure several characteristics like the operation on maximum power point (MPP). On the other hand, The inverter converts DC voltage/current to AC ones thanks to the control circuit which drives switches in such a way as to comply with the international standards, as shown in table 1.1. In PV systems, choppers and inverters are connected in various structures as we find in the literature. In addition, there are many control techniques to connect these DC-DC or DC-AC converters.

Figure1.7 shows a general scheme of a PV system structure. Basically, the system is composed of 4 (four) parts namely: PV group, DC-DC converter, DC-AC converter and a load/grid where:

PV group: The PV group is formed by strings of series and parallel connected panels. The number of panels and the type of connection are chosen following their characteristics (V_{co}, I_{co}, V_{mp}, I_{mp}, ...), the operation power, and also the range of DC voltage level required at the DC-link for DC-AC inverter.

DC-DC converter: There are several types of choppers used with PV systems. Boost converters are usually used when there is a need to increase the input

Table 1.1 – Summary of two standards concern the interconnection of PV systems into grids

Issue	**IEC61727 [18]**	**IEEE STD 1547.2 [19]**
Nominal power	10 KW	30 KW
Voltage for normal operation	85% - 110% (196 V- 253 V)	88% - 110% (97 V- 121 V)
(order-h) limits	(3-9) 4% (11-15) 2% (17-21) 1.5% (23-33) 0.6%	(2-10) 4% (11-16) 2% (17-22) 1.5% (23-34) 0.6% >35 0.3%
Maximum THD	5%	
Power factor at $\frac{1}{2}$ nimial power	0.9	-
Frequency range	50± 1 Hz	59.3 Hz- 60.5 Hz

voltage to higher values for the DC-link. Whereas, Buck converters are used when the voltage of the PV strings is enough for the requirements of the DC-link. The DC-DC stage is used generally to track the MPP by means of many classic tracking control methods such as perturb and observe (PO), incremental conductance (Inc-Cond), Hill Climbing (HC), and many other advanced algorithms.

DC-AC: The inverting stage converts the DC energy to AC one. As explained nextly, there are various topologies that permit the conversion from direct to alternative current. In Chapter 4 a proposed topology called WT-type with better performance is presented and studied. Moreover, different control and modulation strategies to control the power converter, among them FS-MPC control, are presented.

Load/Grid: Depending on the type of load, PV systems are distinguished into 2 types. In this regard, we have grid-connected PV systems if the load is a grid, and off-grid PV systems if the load is a passive load, like for example the rooftop PV systems.

1.6.4 Structures of PV systems

In the previous section, we explained the different parts of PV systems. According to how these parts are connected to each other, we distinguish several structures and

forms. These structures were developed over time to give 4 types as depicted in Figure 1.8. Figure1.8a illustrates the past topology which is called centralized structure. It

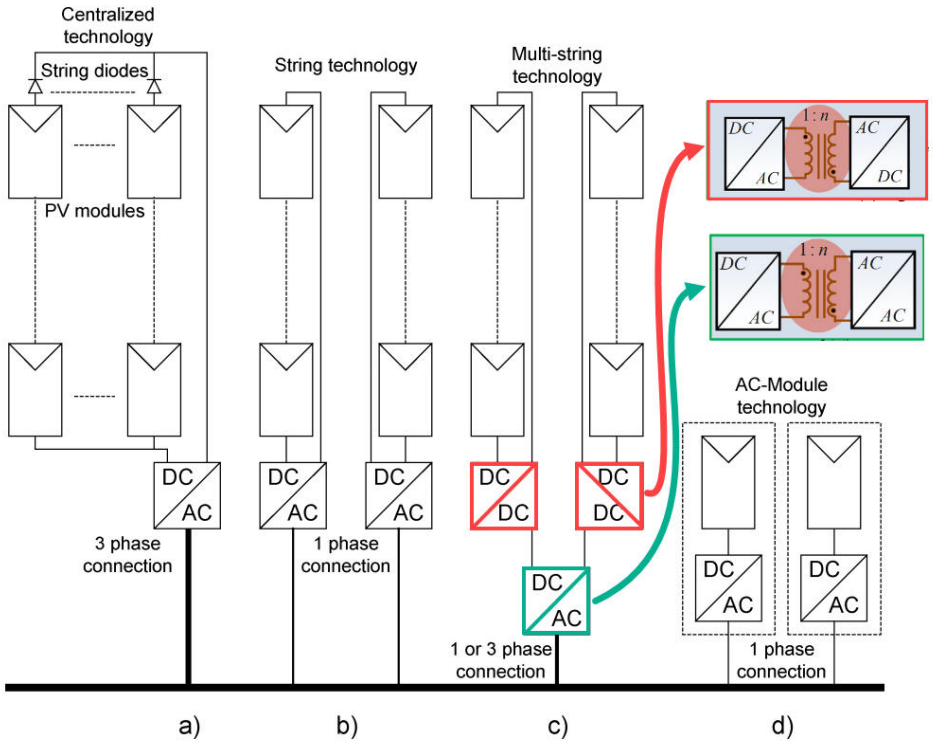


Figure 1.8 – Historical overview of PV inverters. (a) old centralized technology. (b) actual string topology. (c) Present/future multi-string topology. (d) Present/future microinverter topology.

was based on one centrelized inverter that connects the PV group (DC side) to the grid (AC side). The PV group consists of multiple strings, which in turn constitute several series-connected PV modules. The goal of the series connection of panels (strings) is to generate a higher voltage sufficient enough to avoid using transformers for amplification. If we desire to elevate the current we connect several strings in parallel through bypass diodes. [20]

Figure1.8b shows the present structure which is the string inverter structure. It can be considered as a reduced version of the centralized structure, In this structure each PV string is connected to its proper inverter. The suitable operation voltage range for this structure is around 450V-510V. This value can however forgo to higher values as much as 720 V. In some cases, this structure offers the possibility of using a transformer for voltage amplification if the generated voltages are low.

The multi-string structure is depicted in Figure1.8c. The multi-string structure is the development of string inverters structure (Figure 1.8b). It involves the integration of the DC-DC converter to each string. The set of strings is then interfaced with the grid using

one common inverter. This structure offers optimal adjustment between the inverter and PV module since the MPPT is extracted from each string separately. Separated MPPTs can be applied which helps to reduce the price of electricity for mass production. This increases the overall efficiency. Furthermore, this structure facilitates the possibility of enlarging the system's power capacity.

Finally, Figure1.8d shows a PV panel connected to a DC-DC cascaded with a DC-AC inverter in one device. The DC-AC device ensures alternating current at the panel output, in addition, it guarantees MPP operation of each panel thanks to the integrated DC-DC converter as depicted in Figure1.7 [21]. This type of topology is commercialized and found in some applications such as rooftop PV systems. One of the major benefits is effective MPP extraction compared to the multistring structure particularly under shading conditions, the flexibility of the design, and the high efficiency that can be achieved [22]. In the paper [23], researchers analyzed in detail multiple commercial microinverters in terms of operation principle and topological structure.

We can find multiple forms for each of the aforementioned topological structures. For example, the conversion parts: DC-DC and DC-AC as highlighted in red and green colours in Figure1.8 [24] may include the usual Boost/Buck converters or Flyback and Forward converters. These systems may include Line Frequency Transformers (LFT) or High Frequency Transformers (HFT). Figure1.9 shows 2 schemes of industrial PV systems which include the 2 types of transformers: PV system with a high-frequency transformer in Figure1.9a, and a PV system with a low-frequency transformer as shown in Figure1.9b. These two types of transformation are explained in detail in [25]. Meanwhile, Figure1.10 makes a comparison among the efficiency of each type of conversion, which shows that transformerless systems have the best efficiency, after that comes HFT followed by LFT mainly due to transformation losses. P_{DC} refers to direct current power at the input of the inverter, and P_{DCN} is the nominal input power of the inverter.

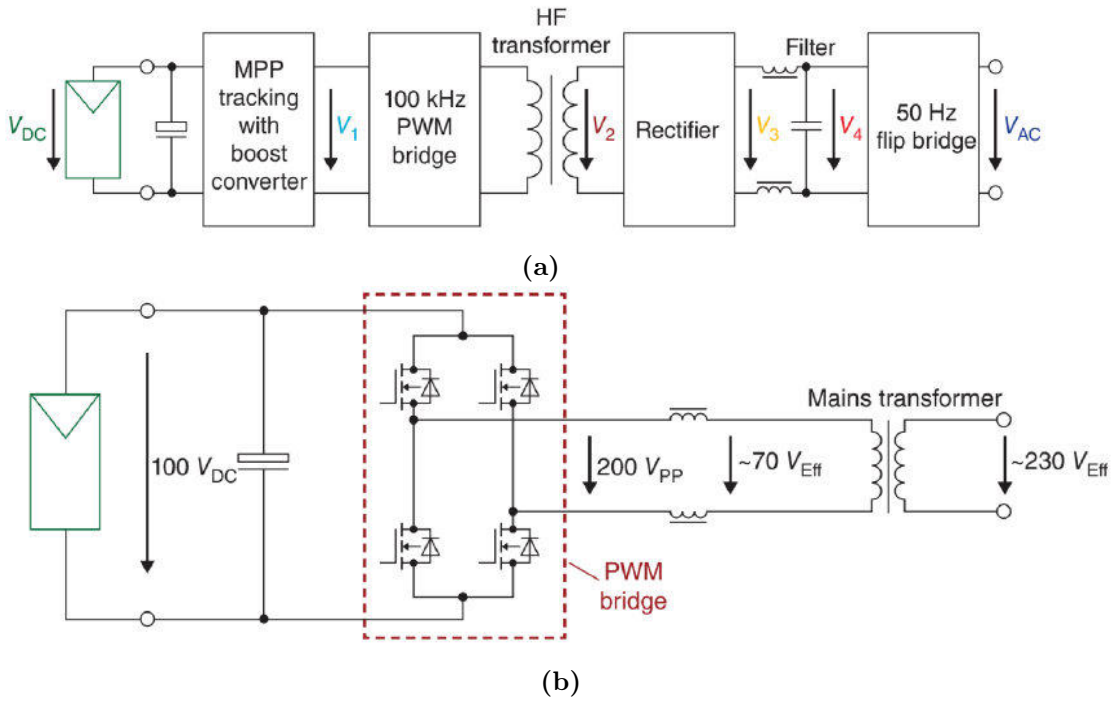


Figure 1.9 – Principle working of PV system with HF transformer (a), PV system with LF transformer (b), Figure source: [25].

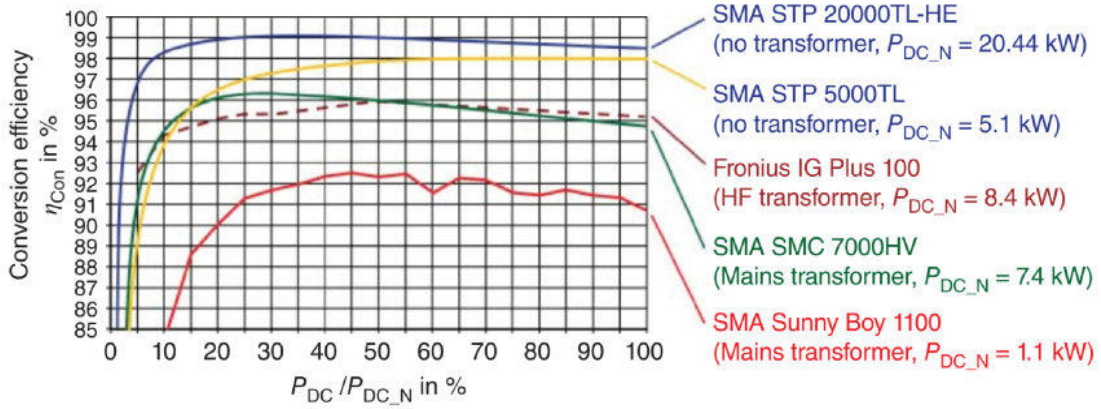


Figure 1.10 – Power conversion efficiency in PV systems with various conversion types with HFT, LFT, and without transformer. Figure source: [25].

1.7 Basics of PV systems plants

Because the primary goal of renewable energy systems is to provide electricity through power plants, the revenues of renewable energy power plants (PV, wind turbine, . . .) come from the sale of electrical energy. This fact drives us to introduce concepts to quantify and

assess the produced electricity. Therefore, to understand the basics about the operation of power plants we need to understand the various factors that help to assess plants and renewable energy systems.

1.7.1 Energy and Power

In power plants, power is seen as the quantity that measures the speed or rate at which energy transfers occur, whereas energy refers to the quantity of energy transferred from a supply source. To understand that, a quantity of energy of 1 Wh does not have to be only provided by supply with a power of 1 W over 1 hour. In other words, the same quantity (1 Wh), can be delivered by a 2 W power supply over 30 minutes. Or by a 0.5 W supply over 2 hours and so on. Figure1.11 some of the systems and the scale of power they consume.

Figure 1.11 – Power rates scale of different devices and systems.

1.7.2 Capacity factor

Renewable power plants can never reach or be close to 100% of their capacity because sun and wind for example are not always available. Therefore, "capacity factor" is introduced which is a variable directly related to the energy source's availability at a specific site, and it is the ratio between the real output of the plant in a period of time (typically a year) over its theoretical capacity: for example a 500MW PV plant that generates 2 GWh a year, have a capacity factor of 45%, as shown in equation 1.1 [26]:

$$\frac{2GWh}{36524h500MW} = \frac{2GWh}{4.83GW} = 0.45 \tag{1.1}$$

A higher value of capacity factor indicates a sunnier or windier site. Besides it indicates the financial viability of the existing or new project. For example, viable onshore wind projects typically refer to capacity factors of 25% to 45%. Meanwhile, for large-scale solar plants a viable capacity factor is between 20% to 30% [27]. Figure1.12 illustrates the capacity factor of various categories of renewable energy plants.

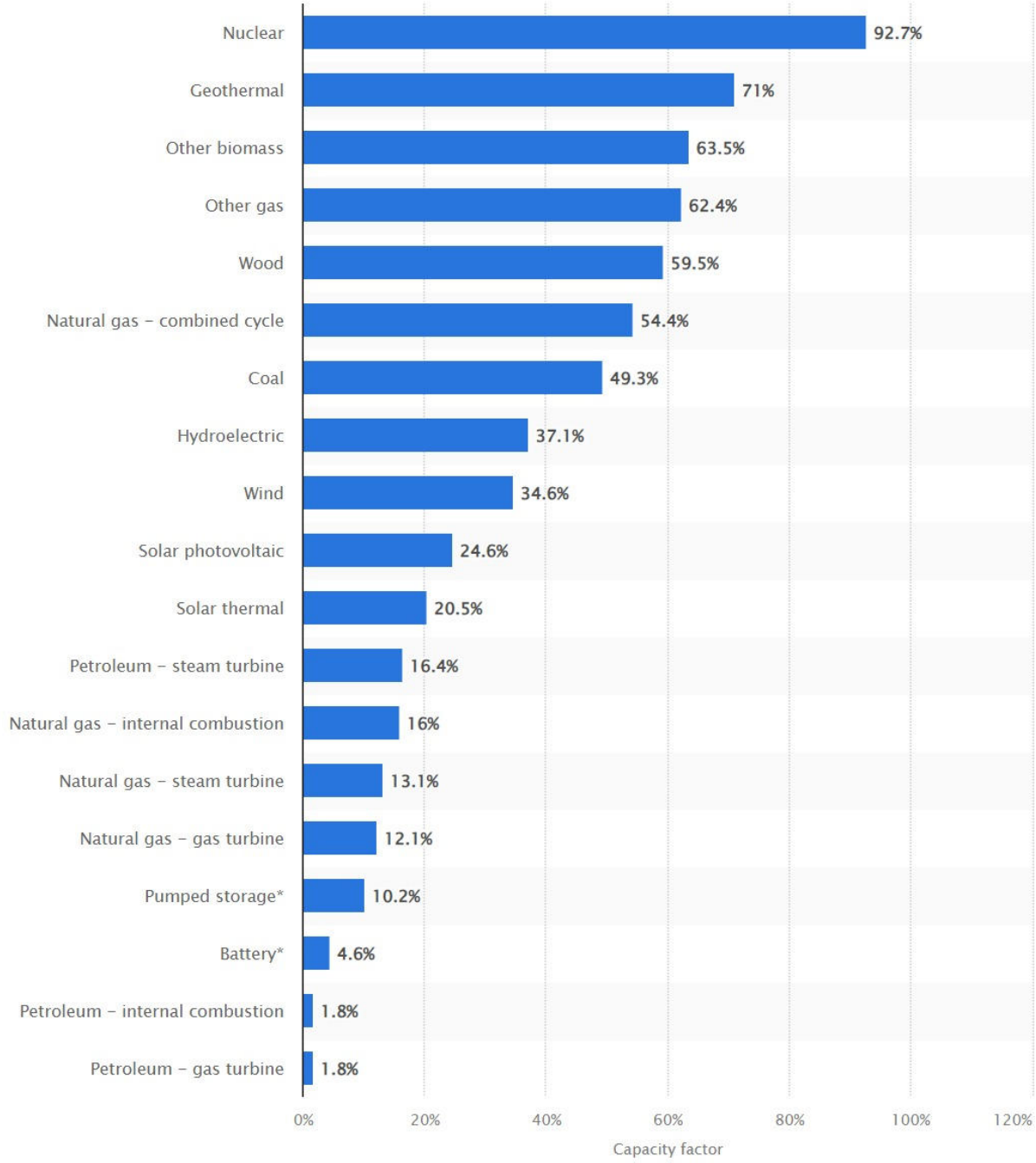
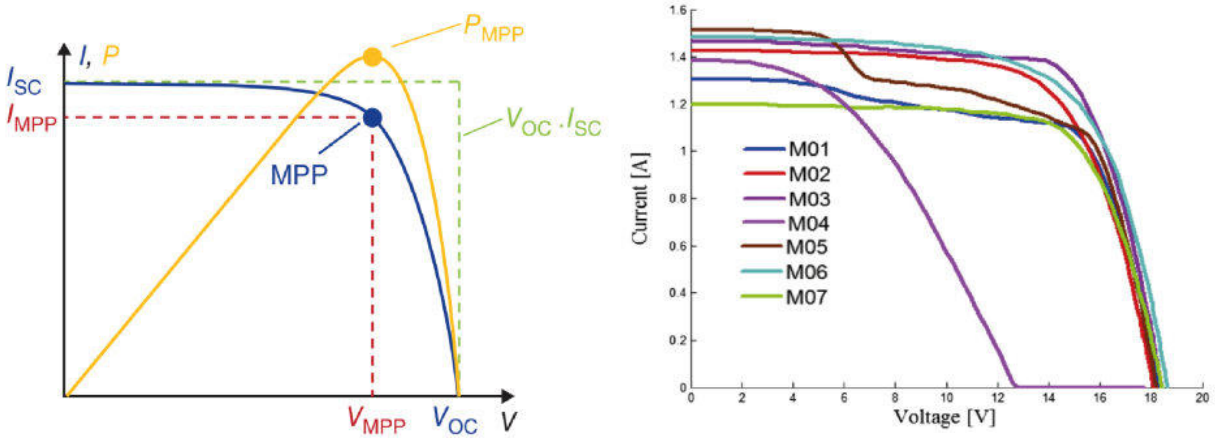


Figure 1.12 – Capacity factor values range of various renewable energy sources, illustration source: [28]

1.7.3 Fill Factor (FF)

The fill factor (FF) is an evaluation entity for PV panels. Its expression is described as a function of MPP power, open-circuit voltage V_{oc}, and short-circuit current I_{sc}. A solar cell (panel) with certain values of V_{oc} and I_{sc} has its unique I-V curve. The fill factor



(a) (b)

Figure 1.13 – The fill factor characteristics (a), Average I-V characteristics of 7 PV modules based on experimental data (b), Figure source a [25], b [30].

measures how much the I-V curve is "square", i.e. how much the I-V curve characteristic approach to the dash line square highlighted in green Figure1.13a. The more the I-V characteristic is square the higher V_{mp} and I_{mp} we get. Moreover, FF helps measure the health of PV panels. As shown in equation 1.2, FF is a portion of Vmp Imp over Voc Isc :

$$FF = \frac{V_{mp}}{I_{mp}} = \frac{V_{oc}}{I_{sc}} \tag{1.2}$$

The FF value of a healthy PV panel is within an interval depending on the technology, where Mono-crystallin Silicon technology has an acceptable range of: 0.80 – 0.85. Meanwhile, the range for Multi-crystallin Silicon technology is 0.75 – 0.80. The lowest FF possible of any technology is 0.25 which is possible to happen due to very significant degradation. Figure1.13b shows the I-V curve of 7 solar panels after 28 years of exposure to weather conditions in Adrar southern Algeria, in a research carried out in 2015 [29]. The curves were acquired through on-site outdoor measurements, each module is named M01, M02, ... M07. As the study concluded, panels with severe degradations are those with an I-V curve less square and hence with a lower FF factor.

1.7.4 I-V characteristic

The I-V curve presents the non-linear variation of current as a function of voltage. it shows the relationship between the flowing current and the voltage generated by the cell/panel and also the nature of this variation. It is worth mentioning that the I-V curve is not restricted to photovoltaic panels, in fact, I-V curves describe the characteristics of any electronic component, namely: motors, resistors, or transistors [25]. Figure1.14

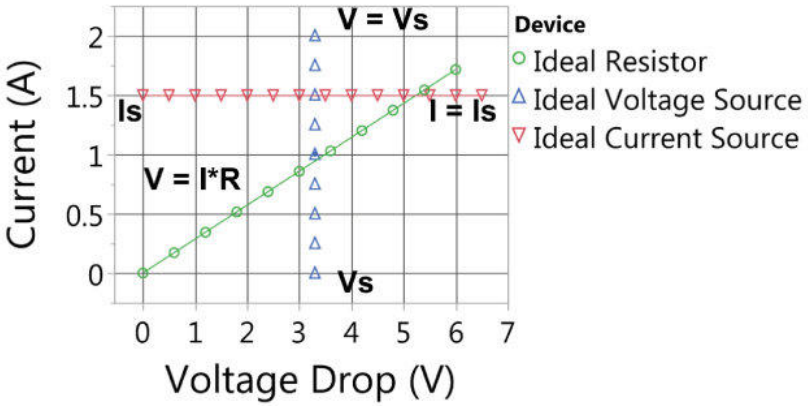


Figure 1.14 – I-V Characteristics of an ideal resistor, ideal voltage source and ideal current source.

depicts three cases of I-V curves.

The I-V curve in green is of a resistor which shows a linear relationship between the applied voltage and the flowing current based on Ohm's Law. The I-V curve in blue presents an ideal voltage source, whereas the curve in red is of an ideal current source. The ideal voltage source generates a constant voltage to the load regardless of the current drawn from it. Conversely, the ideal current source in red provides a constant current regardless of the voltage applied in the circuit.

Speaking of a PV panel, a cell is made of a p-n junction, therefore, it can be considered as a p-n junction of a diode. Thus, the I-V curve of a PV cell corresponds grandly to that of a photodiode (quadrant 1, Figure1.15).

As shown in Figure 1.15, When the operation point of the PV panel is on the first quadrant, it means that the PV panel operates as a generator. In other words, if we are in quadrant 1, that means that the sunlight is hitting the PV panel and there is a produced power being consumed by the load.

The I-V curves can also be extended to quadrant 2 or quadrant 4 shown in red. Suppose the operation point is on either quadrant 2 or 4. In those cases, the PV panel is acting as a load where: quadrant 2 tells that the cell (panel) is reverse biased, which occurs, for example, during periods of partial shading. Meanwhile, operation in quadrant 4, requires a PV cell to be forward biased in the dark [25].

As shown in Figure 1.16, the three key measured points on the I-V curve of most interest: the open circuit V_{oc} at which current is zero, resistance is very high. Short circuit current I_{sc}, at this point, the voltage is zero and the resistance is zero. Also at the maximum power point MPP, the voltage and current are on V_{mpp} and I_{mpp}. These values are affected by temperature and irradiance. Figure 1.16a shows the influence of temperature where the lower the temperature the higher the values are. It is worth

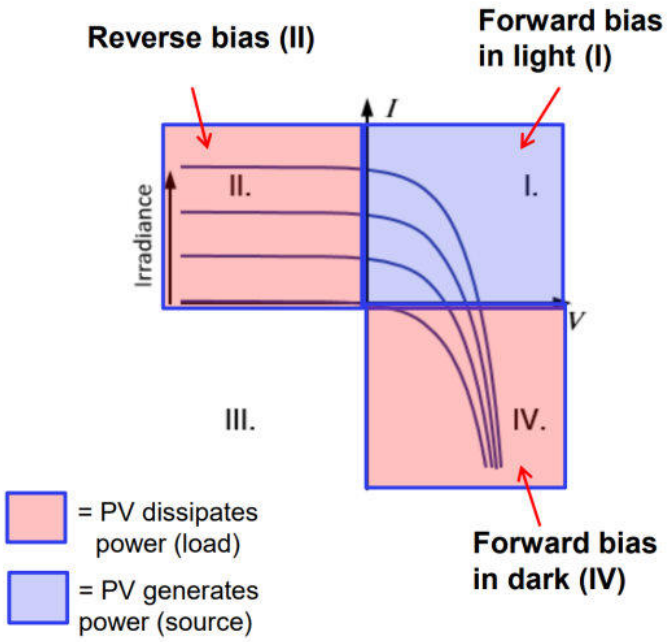
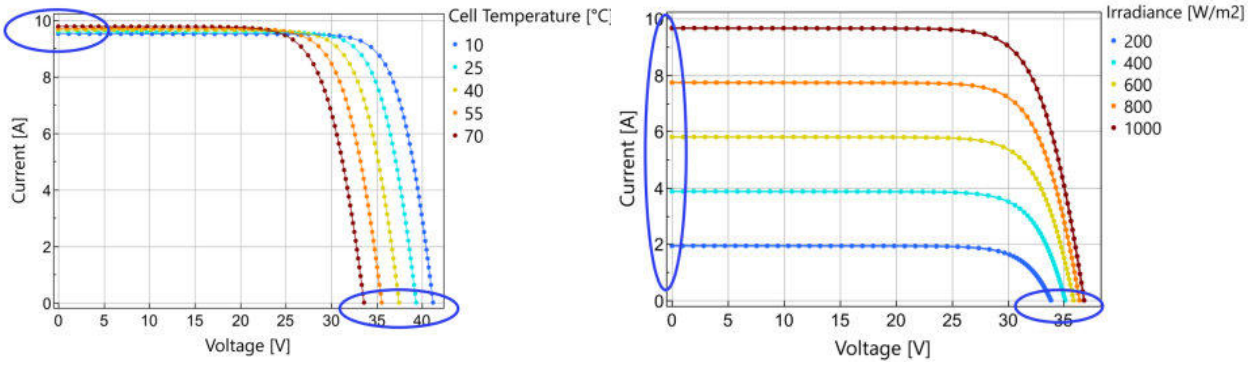


Figure 1.15 – I-V curves of a diode. Quadrant I: The I-V curves of a PV cell.

mentioning that every 1° degree increase above 25° causes a decrease in efficiency η by around 0.5% [31].On the other hand Figure 1.16b shows that as the irradiance increases the values of the previous quantities become higher.

The values of the previous quantities are given in datasheets and are usually evaluated at the common Standard Test Conditions (STC): AM 1.5G spectrum, 1000 W/m², 25 C°.



(a) **(b)**

Figure 1.16 – I-V curves under various temperatures. (a) presents the I-V curves in various Irradiance conditions (b)

1.7.5 Solar cell model

The need for predicting the non-linear output power of the solar cell (PV model) in accordance with the permanent weather variation, leads scientists to design various

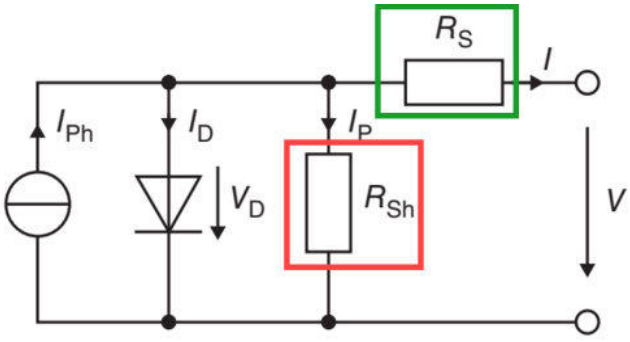
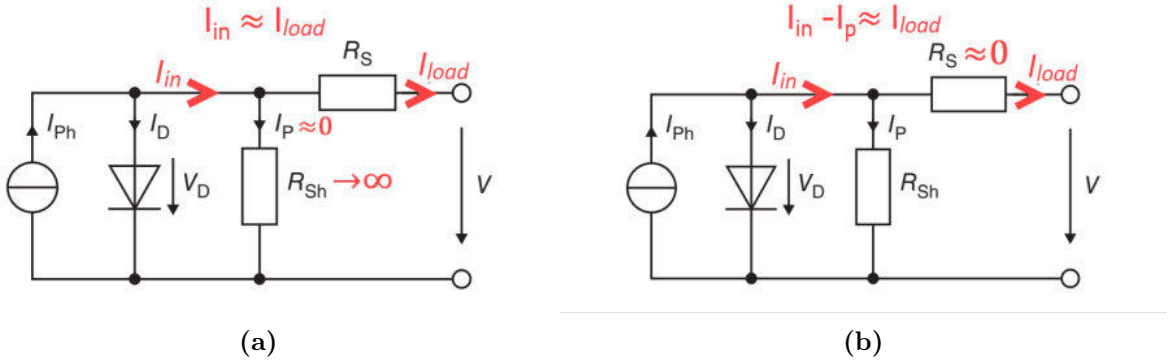


Figure 1.17 – Equivalent circuit for solar cells and solar modules.



(a) **(b)**

Figure 1.18 – Equivalent circuit for solar cells and solar modules and of the influence of R_s and R_sh on the cell/panel considering Ohm's Law.

equivalent models. In the literature, we distinguish 2 types of models:

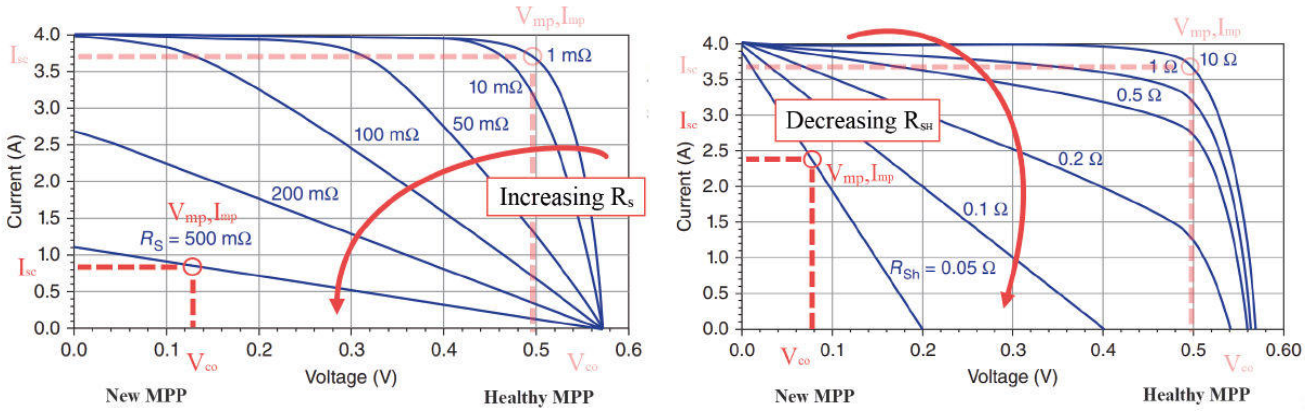
- **Equivalent Circuit models:** permits the generation of a complete I-V characteristic, for instance: 1 diode circuit model 1.17, 2 diode circuit model.
- **Point value models:** this model allows estimate only the prominent points (I_{sc}, V_{oc}, I_{mp}, V_{mp}) on the I-V curve using several techniques, for instance:

— Heydenreich 1 [32].

— Sandia Array Performance Model [33].

— Mechanistic Performance Model [34].

The first model type *Equivalent Circuit model* is discussed. This model contains various forms that describe solar cells, and a simplified model is considered. It consists of parasitic resistances that cause a certain amount of losses. These resistances are series resistance R_s, in green, and shunt R_{sh} (parallel) resistance, which is in red as shown in Figure 1.17. The shunt resistance is called so because it is connected in parallel with the current source and diode, whereas, the series resistance is in series with the load.



(a) (b)

Figure 1.19 – The influence of R_s and R_{sh} on the I-V characteristic of the cell/panel.

We notice from the equivalent circuit model that the series resistance R_s should be low in an ideal solar cell. In fact, according to Ohm's Law, it prevents the current from flowing to the external circuit (load) as shown in Figure1.18a. This resistance is caused by several factors, for example, resistances within the semiconductor and low purity levels of silicon.

On the other hand, if there is current flowing through the shunt resistance R_{sh}, this means that the current issued from the current source (solar cell) is not completely reaching the output load which is undesirable because less current will be delivered to an external circuit. Therefore, we deduct that in an ideal solar cell, parallel resistance should be high as detailed in Figure 1.18b.

These two parameters R_s, R_{sh} are susceptible to degradation over time when PV panels are in operation which causes their values to increase and decrease respectively. Figure1.19a shows the influence of R_s degradation on the MPP of the panel. It is remarkable that the increasing value of R_s results in a curve that is less square (lower fill factor), and therefore, a significant I_{mp} current. Figure1.19b depicts the influence of R_{sh} degradation on the MPP of the cell. A decrease of the R_{sh} results in a lower fill factor, in other words, a significantly lower V_{mp} output voltage of the panel.

1.7.6 Radiation and Irradiation

Solar radiation is the solar power received from the sun per unit of surface (W/m^2) in the form of electromagnetic radiance. Whereas, solar irradiation is solar power consumed over a given time ($Joule/m^2$) or (Wh/m^2). Figure 1.20 depicts the difference between solar radiance and irradiance. The x-axis presents the time and on the y-axis, we have

the radiation from the sun. Before 6 am the solar radiation is zero because it is night. After 6 am the sun's radiation increases gradually until 12 am when it reaches the maximum because the rays are perpendicular to the surface of the earth which gives us the highest radiation. After 12 am the radiation decreases until it becomes zero at 6 pm, which is when the sun's rays are parallel to the surface.

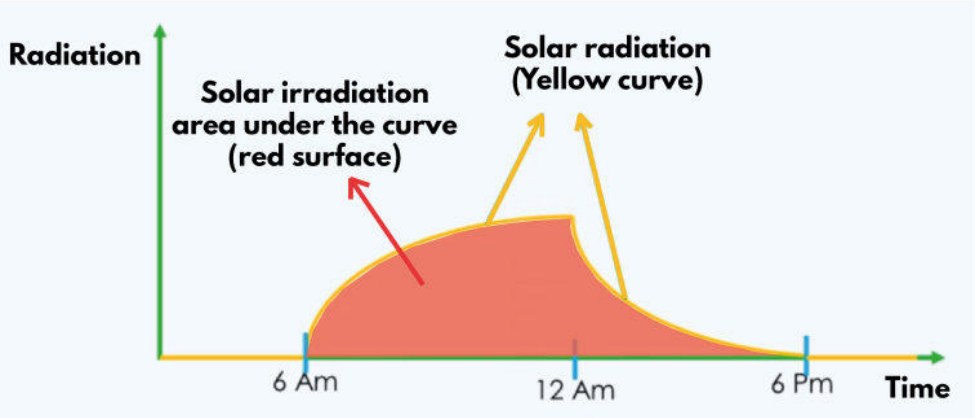


Figure 1.20 – Difference between sun's radiation and irradiation.

One of the unfortunate states of a solar system is the absence of sun irradiation. Nevertheless, solar panels are still able to generate a certain amount of electricity, even when the Sun is not directly shining onto their surface. This is due to the fact that solar irradiance is made up of several components. Therefore, the various components of the irradiance on the array surface which is referred to as Global Irradiance in the Plane of the Array (G_{POA}), are expressed as follows:

$$G_{POA} = G_B + G_D + G_R \tag{1.3}$$

The surface of a solar panel receives irradiance composed of 3 components: G_B direct beam, G_D diffuse beams, G_R reflection beams (from the ground).

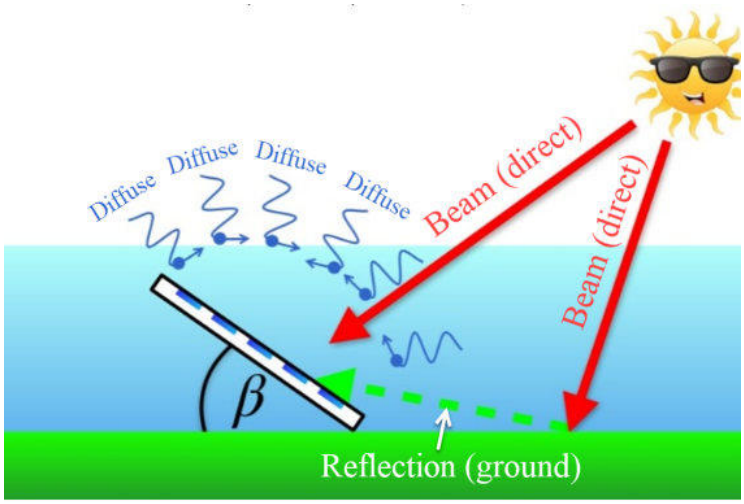


Figure 1.21 – Irradiation on surfaces with tilted angle β: it is composed of direct, diffused, and reflected radiation.

From the illustration 1.21, we notice that diffuse radiation G_D is the part that reaches the most the panel surface which presents a considerable part of radiation. Therefore, even on cloudy days, PV panels are able to generate a considerable amount of electricity. For instance, in Denmark, a cloudy day in summer can provide over 50% of the radiation from a clear sky day [35].

1.7.7 Losses, mismatch problems and bypass diode

1.7.7.1 Losses

PV panels have a low energy efficiency of no more than 25% in general. Hence, it is necessary to transmit the produced energy to the load with as minimum losses as possible. Therefore, it is necessary to eliminate factors that cause losses to occur in PV systems:

(1) **Shading Losses:** It is considered one of the most important factors that significantly affect the performance of PV systems. It may be caused by neighbouring buildings, and trees and sometimes due to some PV panels shading on others, usually called self-shadowing.

(2) **Dust Losses:** These losses are caused by the pollution of PV module surface. In areas with low rainfall rates, these losses can hit 15% of the input energy in extreme cases [36]. To maintain the system's efficiency high, modules need to be cleaned regularly, though, this process may be very costly in the case of a large solar power plant.

(3) **Reflection Losses:** The PV module absorbs solar radiation that hits the surface, in

fact, a certain amount of solar irradiation is reflected back which induces reflection losses. Consequently, modules are usually covered with anti-reflecting films.

(4) **Thermal Losses:** PV cells transform solar radiation into electrical energy, and along with that, it converts a portion of solar radiation into heat, which is not desirable. PV performance becomes poorer with increasing temperatures as seen in Figure1.16b. In addition, the solar energy received on the surface which is not converted by the cell causes heating of the modules and thus more thermal losses.

(5) **Direct Current Cable Losses:** They present losses due to cables that usually connect PV panel to the inverter. The rate of these losses in a well-designed installation does not have to reach 2% at the design of the system and over time due to weather conditions.

(6) **Mismatch losses:** It can be defined as losses caused by the differences of power among the cells of a panel, or among each module in an array [37].

1.7.7.2 Mismatch problems:

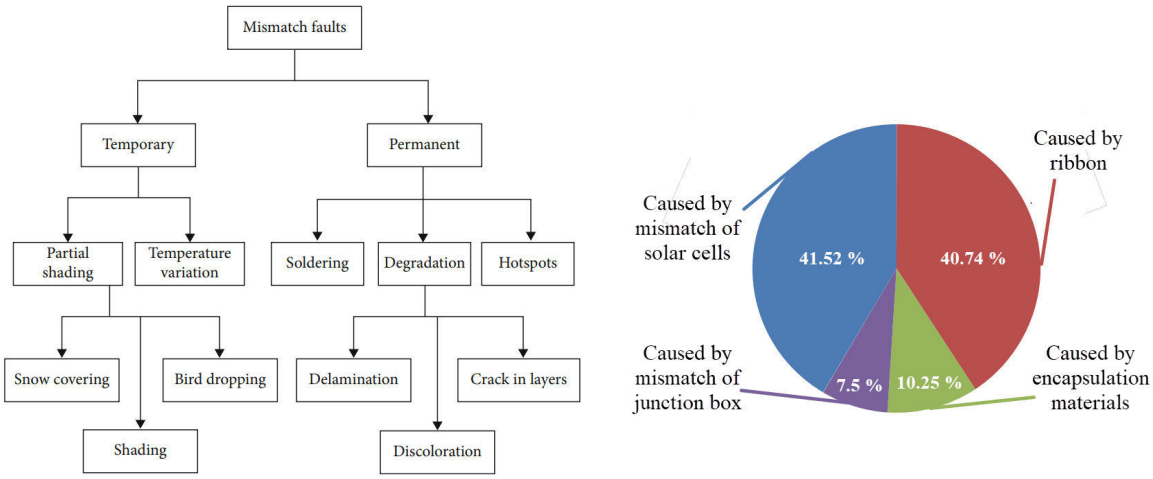
We call mismatch problems issues that occur when the electrical characteristics of solar cells (panels) do not match or are not the same. Figure1.22b shows the distribution of these losses in percentage. Mismatches affect negatively the systems and trigger various types of problems [37]:

(1) **Module Mismatch:** As depicted in Figure1.22a, 1.22b this problem can happen and be permanent if caused by for example hotspot, degradation, soldering, or it can be temporary like in the case of shading and temperature.

(2) **Current mismatch :** Due to their low voltage (0.5 to 0.6 V) and relatively sufficient current (2A/cell), solar cells inside panels are connected in series to reach high voltage. This on the other hand, makes it susceptible to mismatch problems, for example, when one cell is shaded, the current of the entire string is limited by the cell with the lowest current. Even worse, these mismatch losses cannot only occur between cells within a module but also between modules in a string. Meaning that a single shaded cell could severely reduce the power production of the entire PV array.

(3) **Voltage Mismatch:** It occurs when the voltage outputs of cells or modules are different. Which happens usually due to differences in temperature or properties among cells.

(4) **Aging Mismatch:** Solar cells can degrade over time at different rates. This results in a performance mismatch because some cells lose efficiency more rapidly than



(a) **(b)**

Figure 1.22 – Mismatch losses classification in a solar module (a) -Figure source: [37], power loss factors distribution in a solar module (b)-Figure source: [38].

others, therefore, reducing the overall PV system power production.

1.7.7.3 Bypass diode and shading:

Figure1.23 shows the current flow when the panel is subjected to partial shading. When PV1 is exposed to irradiation and generates current, the cells will have a certain amount of voltage which reverse biases the bypass diode d1 and it is in a blocking state. Meanwhile, when PV2 is not generating current or is generating low current, it will apply no reverse voltage (or a sufficient reverse voltage) on the bypass diode d2 as shown in the PV2 loop. The case of PV3 is similar to PV1, the cells generate electricity and apply a reverse voltage on the bypass diode d3.

In this case, bypass diode d2 conducts and segregates the shaded panel/string due to the fact that the cathode of bypass diode d2 receives the voltage of the anode of d3. On the other hand, the anode of diode d2 receives the voltage of cathode d1. As a result, the applied voltage is positive and d2 is forward-biased. If the bypass diode is not connected, the current will pass through the shaded cell which will act like a load, which is the case of quadrant 2 in Figure1.15 as the current has a positive sign +, and the voltage has a negative sign -. [39] [25].

Figure1.24a shows the connection of bypass diodes as they are connected inside PV panels. When the panel is partially shaded, the bypass diode is activated and delists the shaded string to maintain higher power generation. Figure1.24b, depicts an X-ray image of a real solar panel showing 2 bypass diode [40].

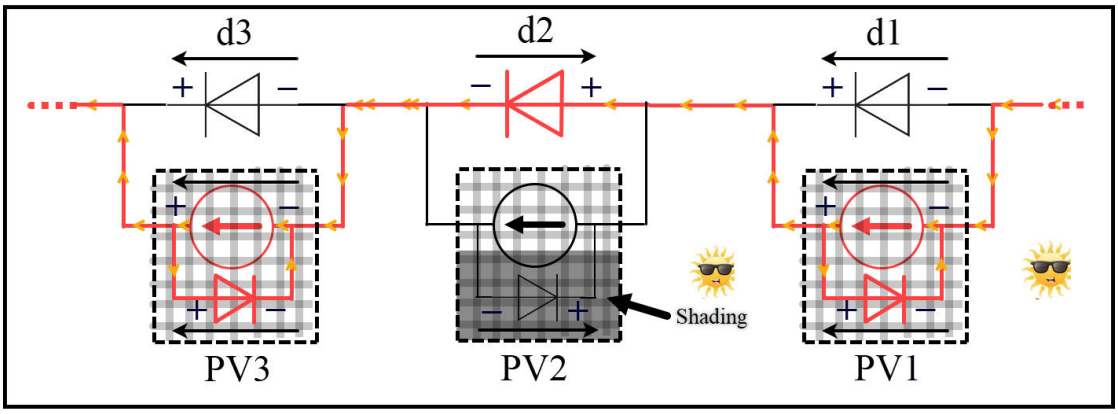


Figure 1.23 – The operation of a PV panel and the flow of current through bypass diode in case of partial shading using an equivalent model according to Ohm's law.

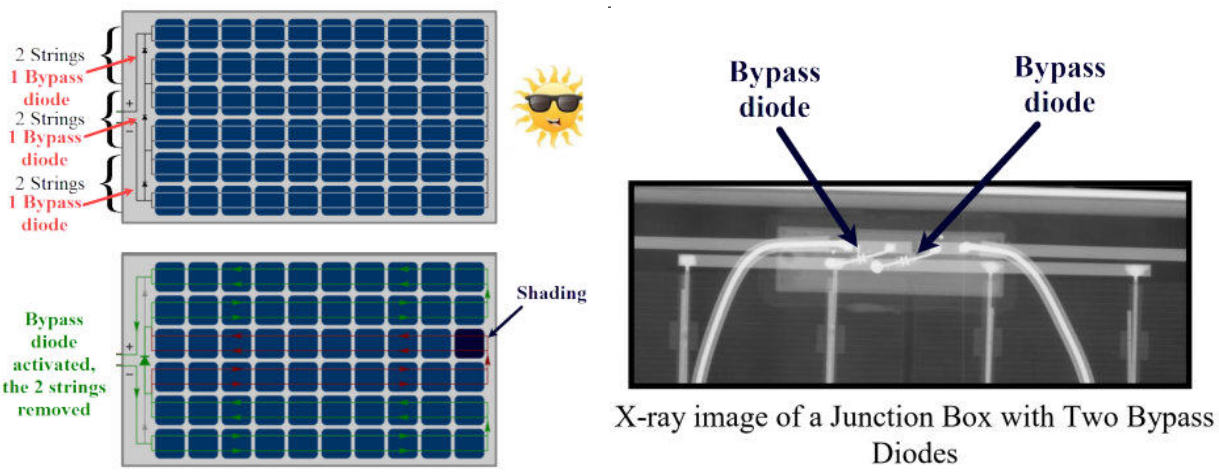


Figure 1.24 – Presents the inner structure of a PV panel showing the connection of bypass diodes with strings.(a), presents X-ray image of the part of the PV panel with bypass diodes, Figure source: [40]

1.8 Conclusion

Renewable energies are necessary for the national security of countries thanks to their availability to all the countries of the globe, and also for protecting our planet. Among the various accessible renewable sources, solar energy gained specific attention in the industrial and academic communities due to its promising potential. We also showed how a little surface in desert regions, like Algeria, can provide the planet with its daily need for electricity.

PV systems developed over time to give better structure topologies for best energy efficiency. We have walked through some basic concepts that help assess and understand power plants, like the difference between power and energy, the capacity factor that gives the real amount of energy expected from the plant, the fill factor that helps in measuring the degradation of PV panels, I-V characteristic, the different models of PV cells that help perfectly plot their I-V curve. Also, we have seen that cloudy days are beneficial to PV systems thanks to the diffusion radiations component which makes an important part of solar irradiation. Finally, we explained in detail how shading affects the working of solar cells and the role of bypass diodes in the mitigation of this challenge.

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Chapter 2

Multilevel inverter topologies and their control

2.1 Introduction

The attention to multilevel inverters has significantly increased in recent years. It is noticeable from the academic production that this area of power electronics is continuously being developed and enriched with novel multilevel inverter topologies and control techniques. The main concept behind multilevel inverters is using switches with limited characteristics to operate at high power rates. Where the high voltages at the input are distributed among all the switches, and every switch withstands a lower value. Therefore, multilevel inverters became an attractive solution for multiple fields in medium (6kV-7kV) voltage as they produce alternative voltage waveform AC very close to a sinusoid by using voltage fragments in the form of staircases. This later results in performance with low harmonics THD, reduced dv/dt and di/dt and reduced electromagnetic interference EMI [1].

Multilevel inverters are considered the advancement of the conventional voltage source two-level 2L-VSI inverter. Therefore, they gradually started to find their place in the industry and substitute 2L-VSI. Multilevel inverters are found in various industries such as current transmission systems FACTS, battery energy storage systems BESS, uninterrupted power supplies UPS, adjustable speed drives ASD, electric vehicles EVs, photovoltaic systems PVs, transmission high-voltage direct current HVDC and wind turbine energy systems WT.

As mentioned above, multilevel inverters use various components connected in a specific way. The manner of this connection is what defines the type of the multilevel inverter. In this context, many circuits were introduced from which we distinguish conventional

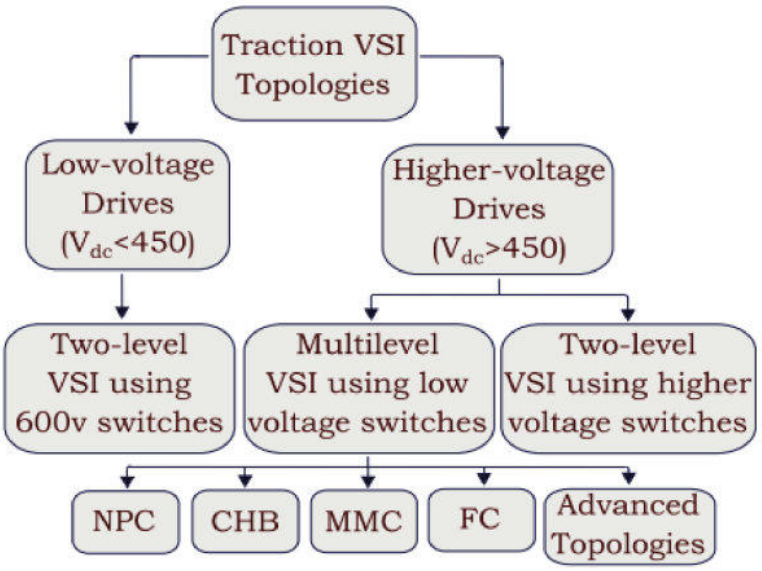


Figure 2.1 – Classification of topologies as a function of operation voltage range, Figure source [5]

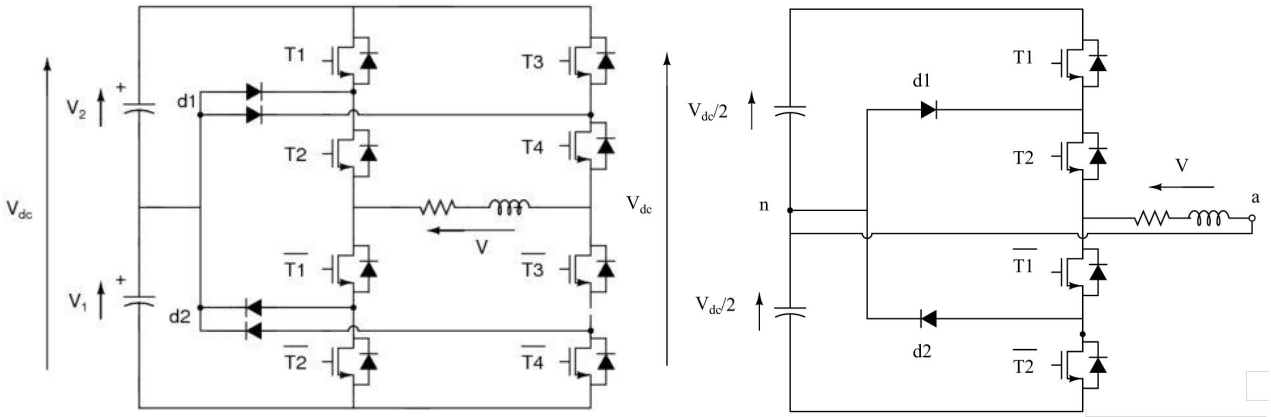
topologies like Neutral point clamped NPC [2], flying capacitor FC [3], modular H-bridge MHB [4], as well as other emerging topologies that attempt to deliver cost-efficient circuits, better quality of output energy, higher power density also with simple control circuits.

2.2 Multilevel inverter topologies

2.2.1 Diode Clamped Multilevel Inverter (DC-MLI):

Three-level neutral point clamped NPC is the simplest version of the Diode Clamped-MLI (DC-MLI). It was revealed in 1981 by Nabae and al [6]. The concept of this inverter is simple, in a 3-level circuit of this topology, the input DC-link voltage is divided on the two capacitors c_1 and c_2. These two resulting voltages are used to produce an output voltage of three levels V,0, -V. Breaking down the DC-link voltage into small values of voltage gives the possibility of using the same components of 2L-VSI at higher voltage rates. The point between capacitors c_1 and c_2 is the called neutral point. Diodes d_1 and d_2 clamp the switches to the input voltages [7]. To calculate the number of capacitors needed c, for n level we apply the following formula:

$$c = n - 1 \tag{2.1}$$



(a) (b)

Figure 2.2 – Power circuit of a single phase three-level NPC inverter.

Table 2.1 – Switching states and their corresponding voltages of inverter in Figure 2.2a

T1	T2	T3	T4	V
1	1	0	0	+Vdc
1	1	0	1	+Vdc/2
0	1	0	1	0
0	1	1	1	-Vdc/2
0	0	1	1	- Vdc

Table 2.2 – Switching states and their corresponding voltages of inverter in Figure 2.2b

T1	T2	V
1	1	+Vdc/2
0	1	0
0	0	-Vdc/2

The number of switches per arm is given by:

$$s = 2(n-1) \tag{2.2}$$

The number of clamping diodes d per arm can be deduced using the following expression:

$$d = (n-1)(n-2) \tag{2.3}$$

NPC can be found in two configurations as shown in Figure 2.2. It can be designed based on a full-bridge as shown in Figure 2.2a [8], also it can be based on a half-bridge as shown in Figure 2.2b [2]. In case (a) the full-bridge NPC can generate 3 levels $\pm v_{dc}$, $\pm v_{dc}/2$ and 0. However, in the half-bridge-based NPC (b) it generates only 2 levels $\pm v_{dc}/2$ and 0. Despite the full-bridge-based structure producing higher levels, it contains double the switch count than the half-bridge-based. Tables 2.1 and 2.2 present the switching states of each of the previous circuits. We included only half of the switches as each two operates in a complementary manner.

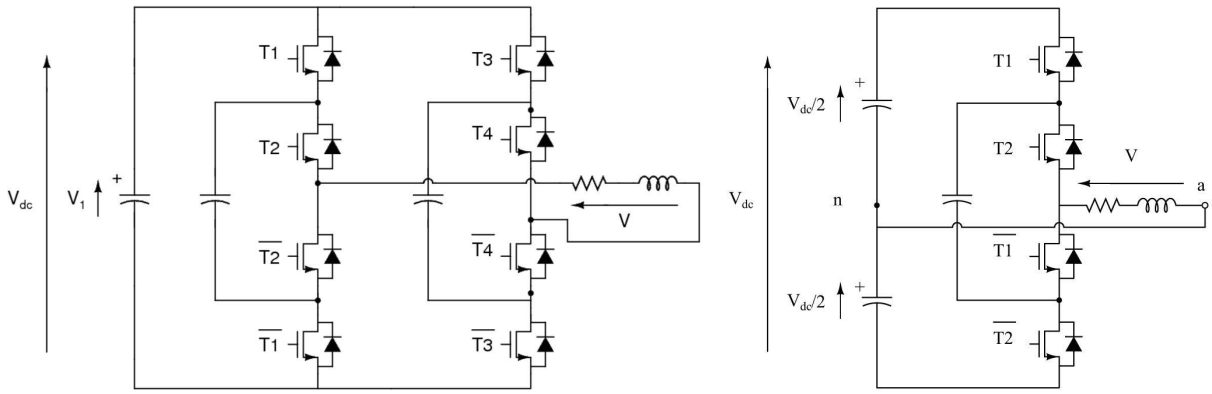


Figure 2.3 – Power circuit of a single phase FC-MLI inverter.

2.2.2 Flying capacitor Multilevel Inverter (FC-MLI):

Flying capacitor inverter was first proposed in 1992 by Meynard and al [2]. The general structure of this inverter is similar to NPC, except that it uses capacitors as clamping elements and is designed based on a basic cell. Clamping capacitors are charged from the DC link input. The inverter follows a pattern of switching to produce the levels V_o, 0, and -V_o. Figure 2.3 shows the topology of a three-level FC-MLI.

Table 2.3 – Switching states and their corresponding voltages of Figure 2.3a

T1	T2	T3	T4	V
1	1	0	0	+Vdc
1	1	1	0	+Vdc/2
0	1	1	1	0
1	0	1	1	-Vdc/2
0	0	1	1	- Vdc

Table 2.4 – Switching states and their corresponding voltages of inverter in Figure 2.3b

T1	T2	V
1	1	+Vdc/2
0	1	0
0	0	-Vdc/2

Likewise, FC can be found in two configurations as shown in Figure 2.3. Depending on the characteristics of the output levels, FC-MLI can be designed based on a full bridge as shown in Figure 2.3a [9], and also can be based on a half bridge as shown in Figure 2.3b [2]. Full-bridge-based FC-MLI (a) generates 3 levels $\pm v_{dc}$, -$\pm v_{dc}/2$ and 0, while the half-bridge based FC (b) generates only 2 levels -$\pm v_{dc}/2$ and 0. As in the previous case, the full-bridge-based structure produces higher levels but it includes double the switch count. In addition, the full bridge FC circuit includes only a single capacitor at the input. Table 2.3 and table 2.4 present the switching states of each of the previous circuits, it is worth mentioning that there are many redundant vectors, we took an example for each vector. In the two circuits, every two switches operates in a complementary manner, this

helped in not repeating the complimentary cases.

The number of input capacitors c for n level is issued by:

$$c = n - 1 \tag{2.4}$$

The number of switches s per arm is given by the relation:

$$s = 2(n - 1) \tag{2.5}$$

The number of clamping capacitors C_c in one leg is calculated using:

$$c_c = (n - 1)(n - 2)/2 \tag{2.6}$$

2.2.3 Modular Multilevel inverter (M-MLI):

The modular inverter is based on the concept of connecting in series multiple modules of full-bridge single-phase inverters as depicted in Figure 2.4b. For a basic modular multilevel inverter, a module is a cell formed with a DC source and two switches working in complimentary. For emergent topologies, the module can include various topologies depending on the desired performance. Figure 2.4a shows an example of a three-phase circuit of this topology. Each phase consists of a single module of a full-bridge inverter. This later is fed by a separate DC source for each phase. [7] [10].

Each cell (module) synthesizes three levels of voltage at the AC output V_o,0, or $-V_o$. The number of levels can be determined as a function of the number of cells using the following formula:

$$n = 2c_e + 1 \tag{2.7}$$

Where c_e represents the number of cells connected in series.

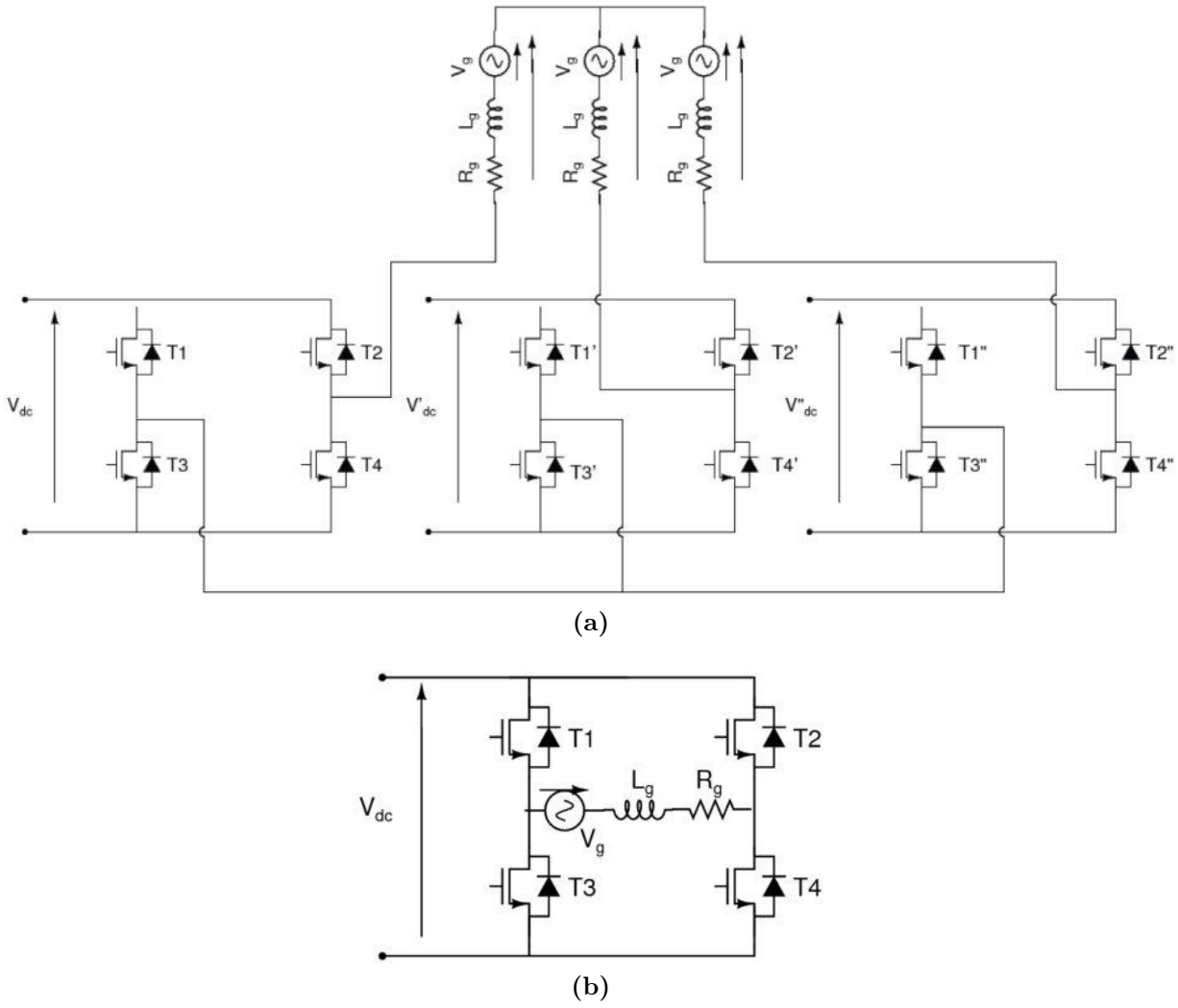
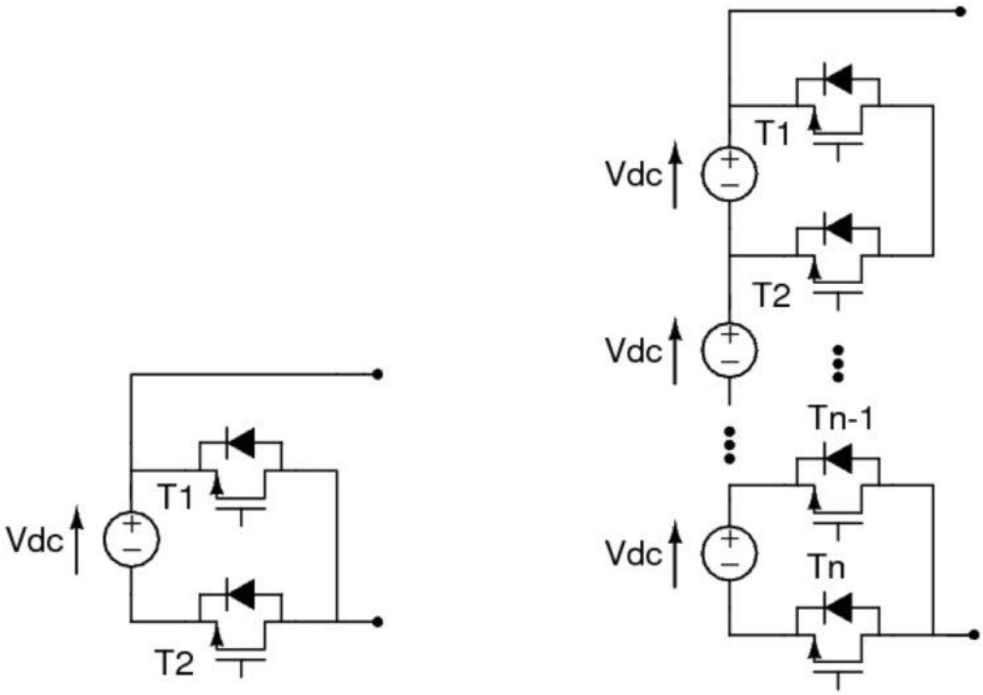


Figure 2.4 – Power circuit of a three-level three-phase M-MLI(a), circuit of a single-phase M-MLI (b)

2.2.4 Reduced switches multilevel inverter (RS-MLI):

Firstly proposed by Babaei in 2007 [11], this topology aims to reduce the number of components used in classical multilevel inverters for better performance and cost-efficiency characteristics. This inverter can operate in symmetrical and asymmetrical modes. Asymmetrical mode means that the levels of the inverter are all equal, whilst, in asymmetrical mode, at least one of the voltage levels is different from the others. The RS-MLI consists of two parts, the first is a level generator while the second part is an H-bridge that assures a negative and positive sign to the levels and also creates level 0. Figure 2.5a shows a basic unit of the voltage levels generator. This unit can be extended to give the general form of this circuit as illustrated in Figure 2.5b [12].



(a) **(b)**

Figure 2.5 – (a) Basic unit of a reduced switches multilevel inverters topology. (b) Extended circuit of reduced switches multilevel inverter.

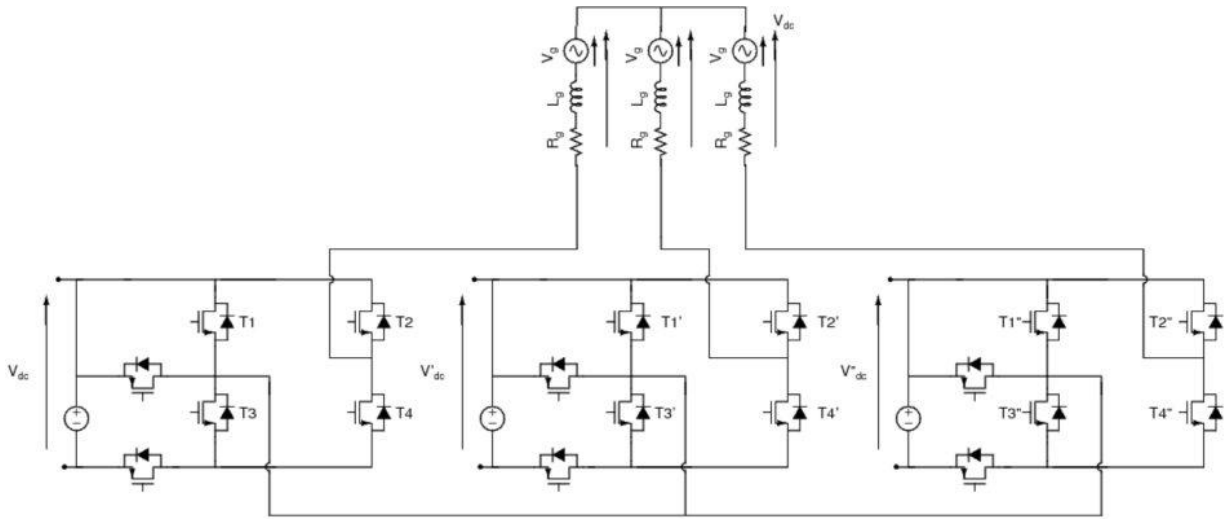


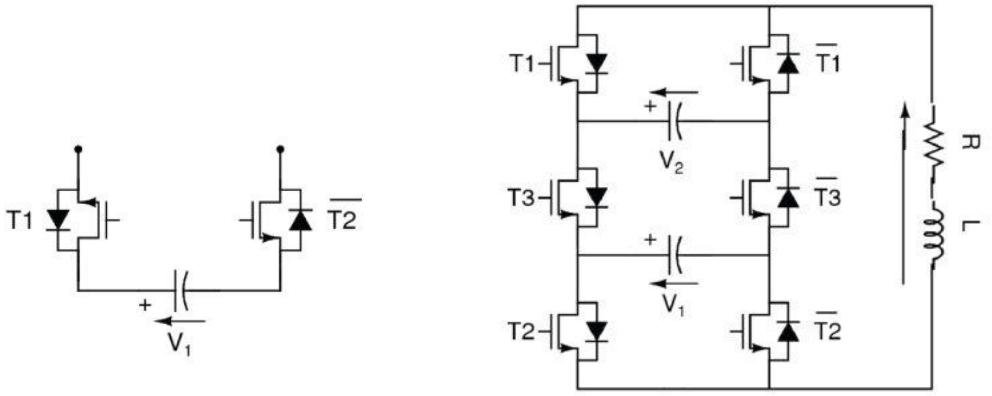
Figure 2.6 – Three-level three-phase reduced switches inverter topology

The number of steps generated by a unit with c number of capacitors is determined by:

$$N_{step} = c(c+1) + 1 \tag{2.8}$$

Table 2.5 – States of switches of the 7-level packed U cell

states	T1	T2	T3
v1	1	0	0
v1-v2	1	0	1
v2	1	1	0
0	1	1	1
0	0	0	0
-v2	0	0	1
v2-v1	0	1	0
v1	0	1	1



(a) **(b)**

Figure 2.7 – A basic cell one source and two switches packed u-cell(a), a seven-level packed U-cell topology (b)

The number of switches used is determined by the following expression :

$$N_{switch} = 2(c+1) \tag{2.9}$$

2.2.5 Packed U-Cell multilevel inverter (PUC-MLI):

Proposed firstly by Ounedjar under the name of a packed U-cell multilevel converter. This inverter is designed based on a cell that consists of a source of voltage and two power switches as shown in Figure 2.7. This converter operates by continuously charging and discharging capacitors. Voltages generated from these capacitors are summed and subtracted in a studied pattern to create various levels at the output as shown in Figure 2.7 and Figure 2.8. Table 2.6 shows the output levels according to the state of switches of the topology depicted by Figure 2.7b [13].

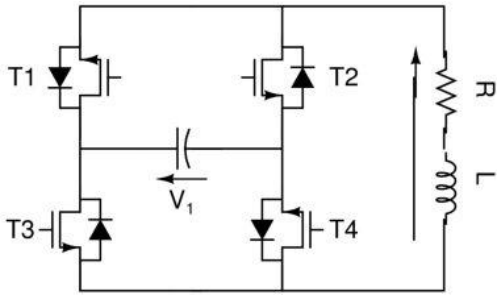


Figure 2.8 – One-phase 3-level Packed U-Cell power circuit.

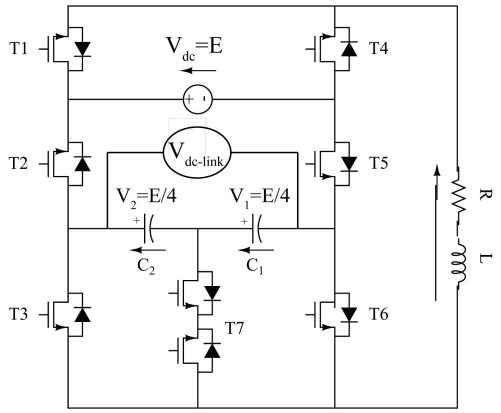


Figure 2.9 – The power circuit of a 9-level packed E-cell multilevel inverter

Table 2.6 – States of switches of the 9-level packed E-cell

states	T1	T2	T3	T4	T5	T6	T7
E	1	0	0	0	1	1	0
$\frac{3E}{4}$	1	0	0	0	1	0	1
$\frac{E}{2}$	1	0	1	0	1	0	0
$\frac{E}{4}$	1	1	0	0	0	0	1
0	1	1	1	0	0	0	0
$\frac{-E}{4}$	0	0	0	1	1	0	1
$\frac{-E}{2}$	0	0	1	1	1	0	0
$\frac{-3E}{4}$	0	1	0	1	0	0	1
-E	0	1	1	1	0	0	0

2.2.6 Packed E-cell multilevel inverter (PE-MLI):

In [14], The PE-MLI is the developement of the previously presented topology PUC-MLI as shown in Figure 2.9. It suggests replacing the unit U-Cell with another unit E-Cell to give better characteristics. This results in a reduction of the number of components for the same levels of output. This inverter enjoys a lot of redundant vectors which help in balancing DC-link capacitors by freely choosing vectors that charge or discharge them

Table 2.7 – Switching states of a single-phase 3-level T-type MLI

Voltage levels	T1	T2	T3	T4	T5
Vdc	1	0	1	1	0
Vdc/2	0	0	0	1	1
0	0	0	1	1	0
-Vdc/2	0	1	0	0	1
-Vdc	0	1	1	0	0

in a symmetrical manner.

The 9-level PEC structure in Figure 2.9 contains 8 switches T_1, T_2, T_3, T_4, T_5, S_7 and a bidirectional one T_6, a single DC source vdc and 2 capacitors C_1 and C_2. The bidirectional switch T_6 is connected to the midpoint of the 2 capacitors. C_1 and C_2 play the role of a second DC-link so that both capacitors can charge and discharge accordingly. As a result, a proper control technique will help to synchronize the voltages that charge and discharge these capacitors to create a balancing state.

2.2.7 T-type multilevel inverter (T-type MLI):

The T-type converter was introduced as an improvement of the classic topologies FC and NPC. Since increasing levels of FC and NPC become a challenge due to the complexity of control, the T-type inverter reduces the cumbersome part and introduces an auxiliary circuit with bidirectional switches [15] [16]. Figure 2.10 shows a 3-level T-type multilevel inverter. An in-depth study about this family is introduced in section 4.2 of chapter 4.

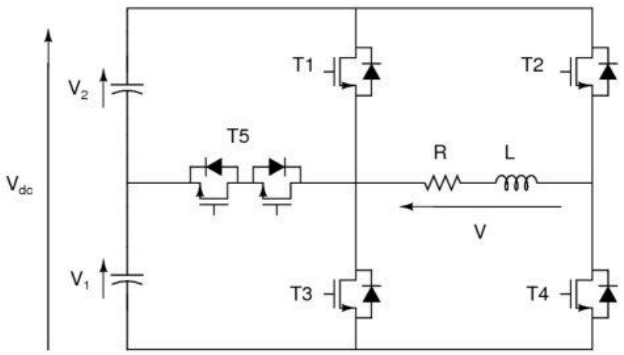


Figure 2.10 – The circuit of a single-phase 3-level T-type inverter

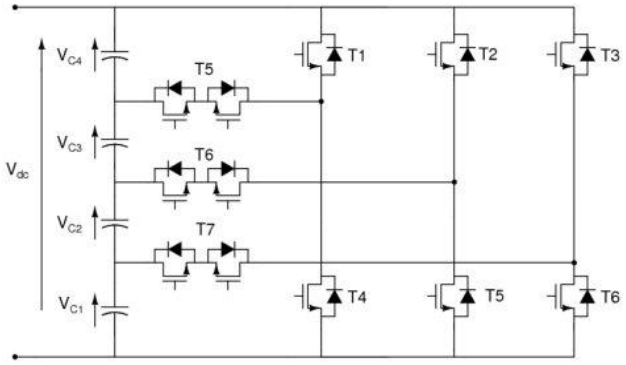


Figure 2.11 – Circuit of a three-phase 9-level T-type MLI

The auxiliary circuit clamps the input DC link to the load using 2 switches. Figure 2.11 presents a 5-level three-phase T-type multilevel inverter. The single-phase topology presented in Figure 2.10, produces 3 levels V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, and $\breve{}V_{dc}$. Table 2.7 explains switching combinations with their corresponding voltages.

2.3 Modulation strategies

2.3.1 Pulse Width Modulation(PWM)

PWM is one of the most known control strategies, it is produced by an intersection of a modulation signal which is usually a sinusoidal curve, and a triangle one. With the introduction of multilevel inverters, the same Pulse width modulation used with the conventional 2L-VSI inverter was modified and extended to suit multilevel inverters. In principle, each triangle carrier refers to a single level of the multilevel inverter. However, this differs from one multilevel inverter to another depending on the topology.

PWM techniques for multilevel converters are classified regarding switching frequency as shown in Figure 2.13. The classical sinusoidal PWM is shown in Figure 2.13a. This later is modified and improved on many levels such as reducing the switching frequency, common mode voltage and maintaining the balance of capacitors. and therefore many other techniques are derived and proposed such as third harmonic injection (THPWM) and space vector SVPWM as shown in Figure 2.13b and Figure 2.13c respectively. The later techniques have the triangular waveform as a common but they differ in the carrier waveform.

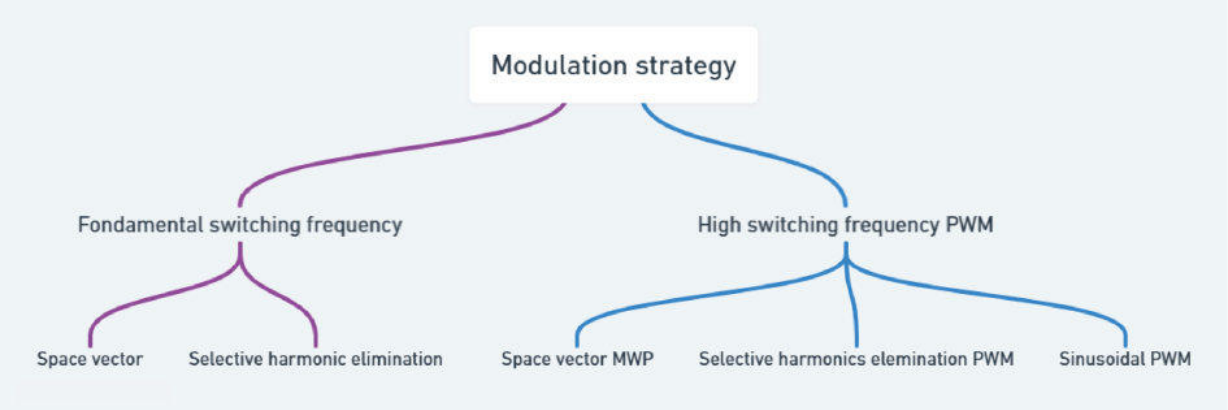


Figure 2.12 – Classification of different PWM strategies

2.3.2 Carrier-based PWM strategy:

Furthermore, other various multicarrier sinusoidal PWM with a distinguished performance have emerged for instance: phase disposition (PD-PWM), phase opposition disposition PWM (POD-PWM), alternate phase opposition disposition PWM (APOD-PWM), and phase shifted PWM (PS-PWM) [18]. These techniques keep the same sinusoidal reference but propose various carrier signals with different displacements. PWM-based control converters are known for their constant switching frequency, however, there are many other PWM-based techniques that result in variable switching operation [19]. The previously mentioned techniques are illustrated in Figure 2.14.

2.3.3 Model Predictive Control (MPC):

Model predictive control (MPC) is one of the prominent advanced modulation and control techniques. This technique is dependent on the model of the system. It uses the dynamics of the system to predict the future possible values with the help of Euler discretization which makes it suitable for numerical application. MPC is simple to implement and can handle multivariable systems with a high-quality performance. Thanks to these advantages, it is applied to many fields of industry i.e. petrochemical plants and vehicle traction..... The advancement of the computational power of hardware such as FPGA and the decrease of sensors cost paved the way for many controls to be easily implemented such as fuzzy, artificial neural network ANN and model predictive control MPC.

In the literature, various MPC techniques have been developed for power electronics control and are classified into two categories: Continuous Control Set MPC (CCS-MPC) and Finite Control Set MPC (FCS-MPC). In the first category, the switching states are

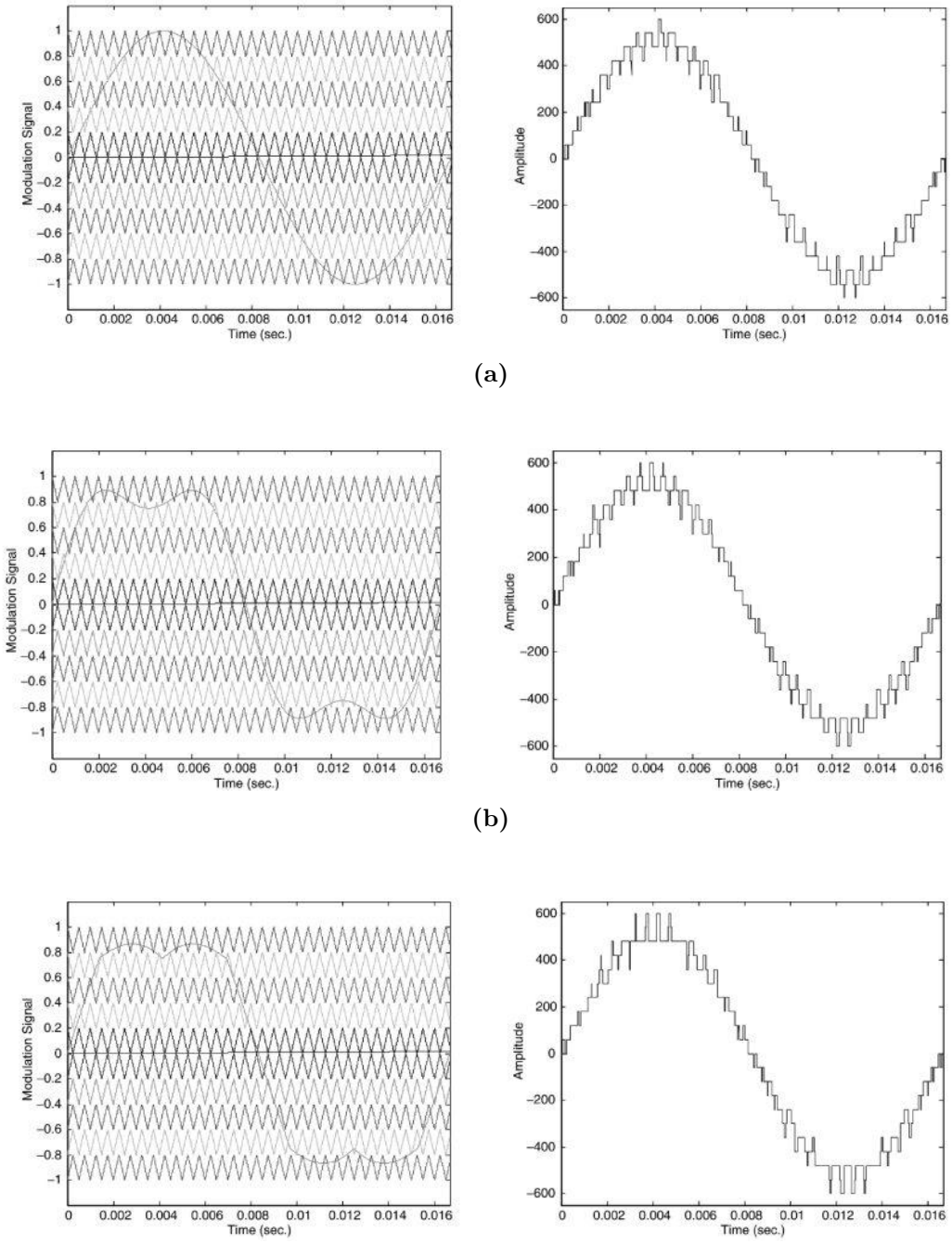


Figure 2.13 – Sinusoidal PWM (a), Third Harmonic Injection (THPWM)(b), Space Vector SVPWM (c), Figure source: [17]

generated by means of a modulator. On the other hand, FCS-MPC solves an optimization problem using the converter's model to generate an optimal set of switching [21].

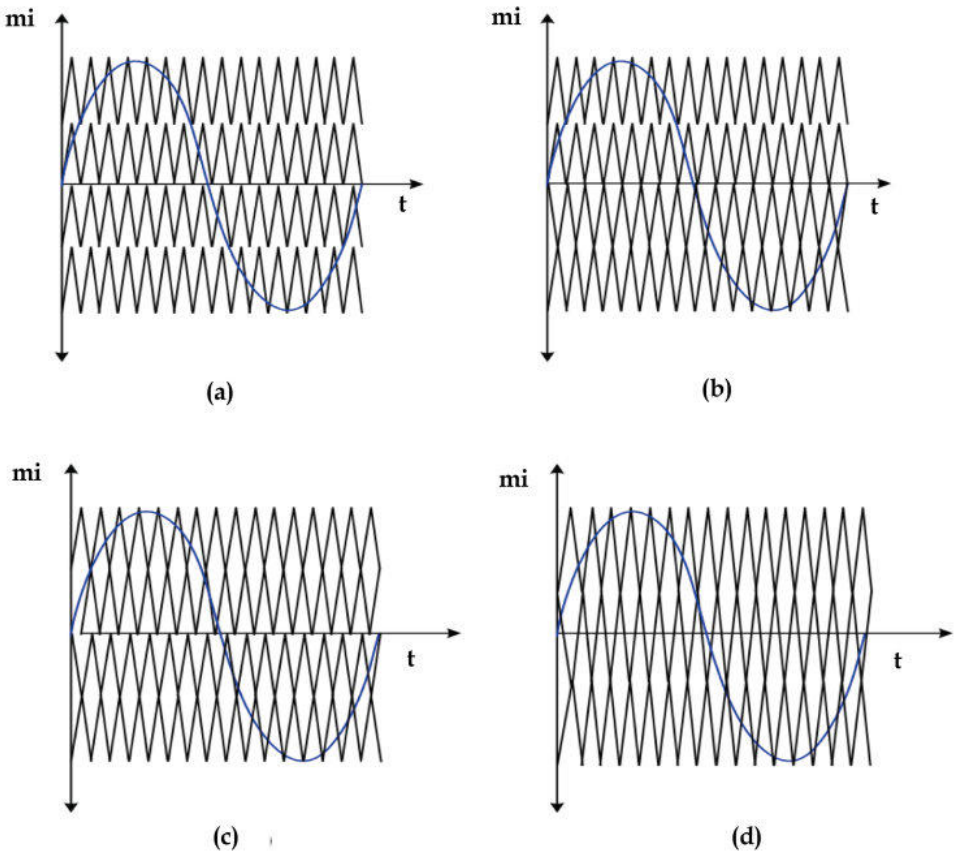


Figure 2.14 – Multicarrier SPWM types: PD(a), POD(b), APOD(c), PS(d), Figure source [20]

2.3.3.1 Emergence of MPC:

The theory of MPC was developed in the 1960s. The presence of this technique in the industry started in the late 1970s when it was successfully implemented in the chemical industry thanks to the low computational burden of this type of system. In the field of power electronics, the early applications return to the 1980s dealing with low-frequency systems. Gradually, higher operation frequencies were performed thanks to the exponential development of microprocessor architecture and power over the last decades. MPC does not present a specific control strategy, in fact, it contains under its umbrella many controllers as shown in Figure 2.17.

2.3.3.2 Operation principle:

The design of a finite set MPC (FS-MPC) is based on the model of the converter. All in all, to design an FS-MPC we follow these steps:

1. Establishing the model of the converter by the identification of all possible switching states. After that, using Ohm's law we define the discrete expression of the load

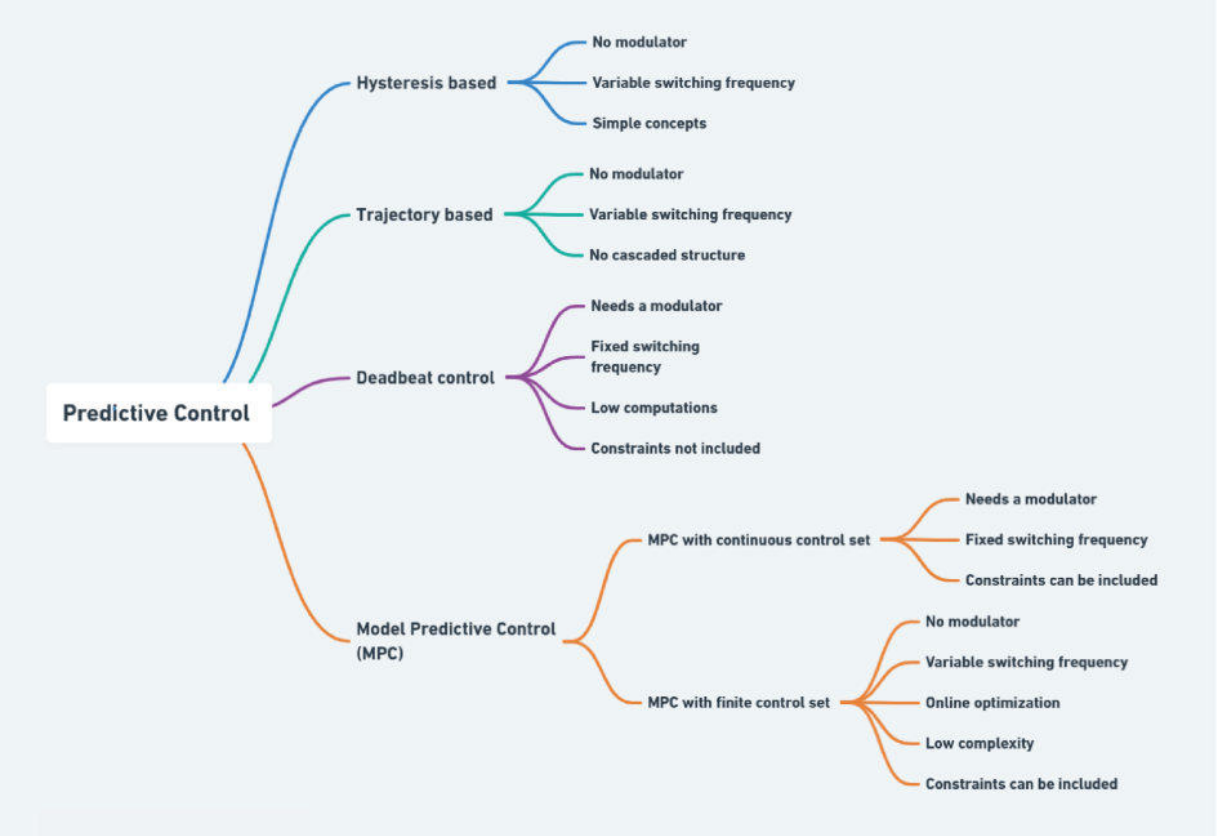


Figure 2.15 – Detailed classifications of families of predictive control

current.

2. Selecting the desired performance of the system and arranging them in a cost function. This later contains reference values that reflect the desired behaviour of the system.
3. The future variables of the system are generated using the discrete-time models built in the first step. These predictions are evaluated by the cost function designed in the second step. The state that responds the most to the desired specifications is applied in the next step T_s.

Based on the method optimization, the MPC family can be classified into two families, Continuous Control Set MPC (CCS-MPC) and Finite Set MPC (FS-MPC). In the first class, the technique relies on a modulation strategy to compute a continuous signal for the switches. The most used techniques of this family are Explicit MPC (E-MPC) and Generalized Predictive Control (GPC). The main advantage of this strategy is the fixed switching frequency. On the other hand, the second class, Finite Control Set MPC (FCS-MPC) directly employs the discrete nature of power converters to develop optimal states, without the need for an external modulator. Also, FCS-MPC is divided into two

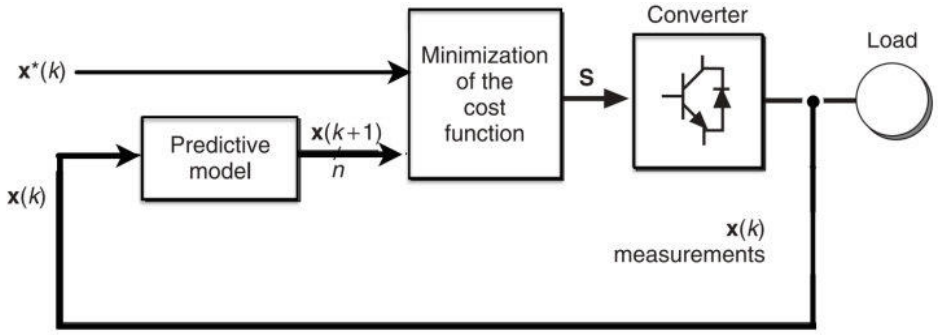


Figure 2.16 – General scheme of MPC control for power electronics

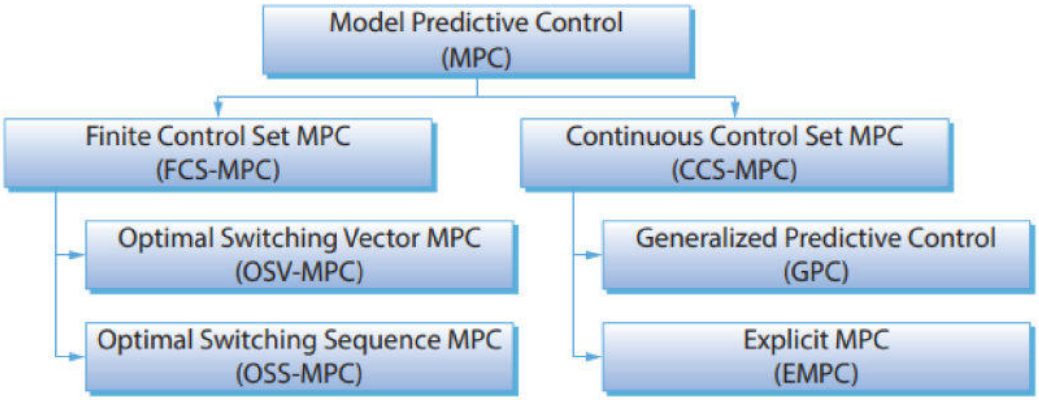


Figure 2.17 – Classification of FS-MPC strategies applied to power converters, Figure source [21]

types: Optimal Switching Sequence MPC (OSS-MPC) and Optimal Switching Vector MPC (OSV-MPC) [21].

OSV-MPC is the first FCS-MPC technique introduced in the literature and is the most popular MPC strategy in power electronics compared to the second class. It uses the output voltages of the converter as the control set and then it finds the optimal Vector predictions for this control set. The main disadvantage of this strategy is the variable switching frequency. In the second type OSS-MPC, instead of considering all possible output vectors as the control set, it instead deals with switching sequences where it calculates the switching sequence that best meets the control objectives at each control cycle. This method of control gives a constant switching frequency. If we compare the two classes, one of the main differences is that CCS-MPC requires less computational capabilities than FS-MPC, due to the fact that this technique performs part of its algorithm offline.

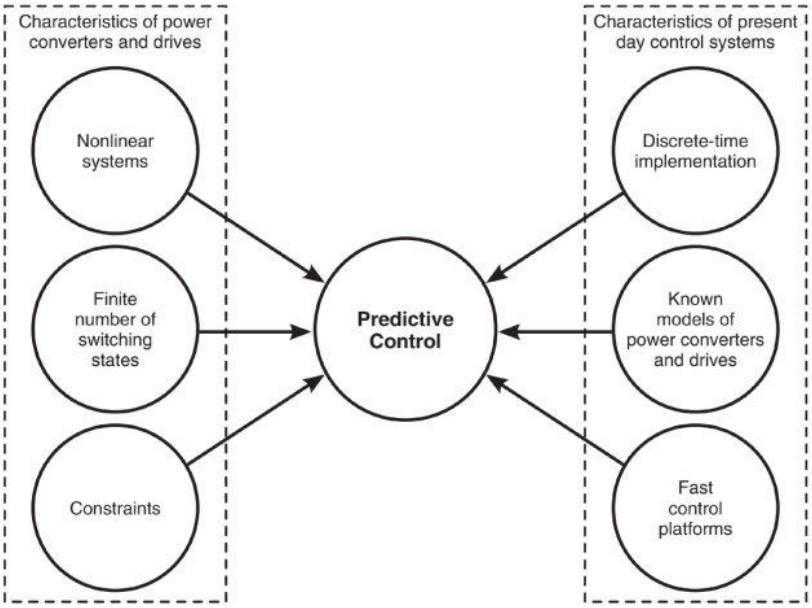


Figure 2.18 – Characteristics of model predictive control [22]

2.3.3.3 Why Predictive Control is Suited for Power Electronics?

Power converters and drives gather various fields of research with the goal of improving their characteristics such as efficiency, Reliability, Harmonic ... etc. These systems combine nonlinear and linear parts and are characterized by their finite number of switching states. The inputs of these systems are discrete and express the two cases: turn on and off of the switches. This binary form of information perfectly matches digital platforms that manage their practical implementations. Recently, control platforms have shown the capability of handling heavy computation control algorithms thanks to the exponential developement of this field. [22]. Therefore, Model predictive control plays a perfect role in matching the natural characteristics of power converters and drives with digital control platforms. As shown in Figure 2.18. As stated previously, MPC technique is a strategy that is based on the mathematical model of the system. MPC uses the dynamics of the systems to predict future values of certain sizes which is carried out thanks to the Euler discretized formula. After that, This technique solves an optimization problem at each step. This optimisation is based on a cost function. This later contains the objectives that reflect the desired behaviour of certain variables. At this stage, the cost function compares all predicted values to the reference at each sampling period. The lowest error responds the most to the desired objective, therefore, to decide which of the possible is optimal. After the optimal state is selected, the algorithm applies it to the load in the next sampling step. To sum up, the design of a Model predictive control is based on three

main steps [22]:

- **Prediction:** MPC technique uses the discrete model of the system to find the value of variables at instant k+1 through numerical iterations. At a fixed prediction horizon and also using feedback measurements of the present values MPC is capable now of determining the future values of the controlled sizes.
- **Optimisation:** The set of predicted values is evaluated using a cost function for all converter vectors. The control technique uses the cost function to determine errors between the reference value and predicted values. These errors indicate how much the predicted value is close to the desired one. A close value means that applying its correspondent vector is recommended. The predicted value that gives the lowest error is chosen and the corresponding voltage vector is thus selected. After the turning on and off states are decided, the control technique applies them in the next step T_s.
- **Feedback:** Model predictive control is a closed-loop control technique, therefore, it needs to use the present values. This process is done through the estimation of the needed values, or simply by a simple acquisition with the help of sensors. As this latter method is costly, the first method is preferred. Much research was proposed to find a way to estimate the needed inputs and get rid of sensors.

2.3.3.4 Mathematical modeling

The model used for prediction is a discrete-time model which can be expressed as a state space model as follows:

$$x(k+1) = Ax(k) + Bu(k) \tag{2.10}$$

$$y(k) = Cx(k) + Du(k) \tag{2.11}$$

The cost function that represents the desired behaviour considers the references and future states:

$$J = f(x(k),\ u(k),\ \dots\ ,\ u(k+N)) \tag{2.12}$$

MPC is an optimization problem that consists of minimizing the cost function J for a predefined horizon N and restrictions of the system. The result is a sequence of N optimal actuations. The controller will apply only the first element of the sequence

$$u(k) = [1\ 0\ \dots\ 0]\ arg\ min(J) \tag{2.13}$$

To get a discrete-time model it is necessary to use discretization methods. For first-

order systems it is useful to approximate the derivatives using the Euler forward method:

$$\frac{dx}{dt} = \frac{(x(k+1) - x(k))}{T_s} \tag{2.14}$$

Where T_s is the sampling time. When the order of the system is higher, Euler discrete-time model becomes less suitable due to the higher error. Therefore an exact discretization technique must be used.

2.4 Model Predictive Control applied to a single-Phase T-type MLI

2.4.1 Introduction:

In power converters, the current is a destructive element, hence, it has been given special attention in control [22]. In this example, the designed FS-MPC control scheme includes a sinusoidal current reference. The designed control is applied to a 3-level single-phase T-type inverter which is a well-known topology that is used in a wide range of industrial applications. The control flowchart is depicted in Figure 4.17.

2.4.2 Finite Set Predictive Current Control FS-MPC:

The 3-level T-type generates a set of finite switching states. This feature enables the FS-MPC strategy to be applied and helps use the models of the multilevel inverter to predict the future behaviour of the load current. The current load is desired to follow a sinusoidal waveform. This objective is expressed within a cost function. After future possibilities are evaluated, FS-MPC selects the state that minimises the error according to the objective, which is applied in the next step of time T_s. We can summarize the steps mentioned above as follows:

- Define an objective value for the cost function g.
- Build the discrete mathematical model of the converter.
- Optimise possible switching states with the cost function.

2.4.3 Cost Function:

As stated before, the cost function consists of the desired reference values. In our case, the desired performance concerns 2 sizes: load current and capacitor balance. Converters are usually found in a three-phase connection or in a single-phase connection. For the

present example, the multilevel inverter is single-phase. Single-phase converters include only one part as shown in equation 2.15 which is the case of the studied inverter, the errors between the reference and the predicted currents are as follows:

$$g = |i(k+1) - i_p(k+1)| \tag{2.15}$$

where i*(k + 1) and i(k + 1) are the reference current and predicted value of current respectively.

In three-phase inverters, a single desired value is usually expressed in two components as shown in equation 2.16. The current is expressed in orthogonal coordinates α and β as reference values as expressed in the following expression:

$$g = |i_\alpha(k+1) - i_{\alpha_p}(k+1)| + |i_\beta(k+1) - i_{\beta_p}(k+1)| \tag{2.16}$$

where $i_\alpha(k+1)$ and $i_\beta(k+1)$ are the real part and imaginary part of the predicted load current i(k + 1). The reference currents $i^*_\alpha(k+1)$ and $i^*_\beta(k+1)$ are the real part and imaginary part of the reference current $i^*(k+1)$.

2.4.4 T-type MLI Model:

The power circuit of the 3-level T-type inverter is depicted in Figure 2.19. Table 2.9 details the output voltages with their corresponding states, while Figure 2.20 illustrates the different modes of the T-type multilevel inverter to generate the output levels. According to Ohm's law, the output voltage of this inverter connected to a resistive load R and inductive load L is given by the following equation:

$$v(t) = R.i_l(t) + L\frac{di_l}{dt} \tag{2.17}$$

Where: i_l: the load current,v: load voltage, R: load resistor, L: load inductance, T_s: sampling time. The discrete form of equation 2.17 after Euler discretization is given by equation 2.18:

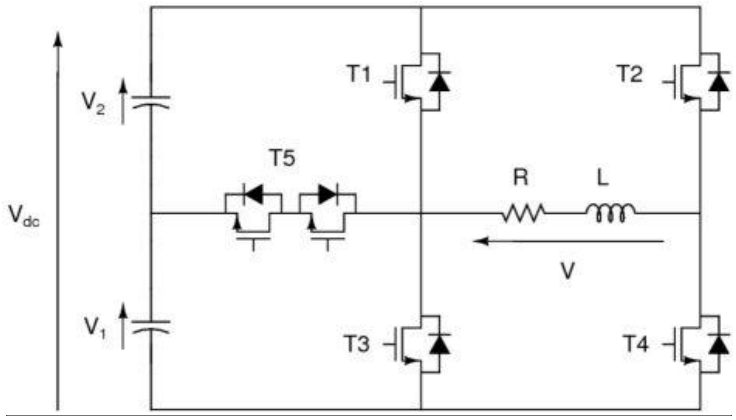


Figure 2.19 – The Circuit of a 5-level T-type multilevel inverter

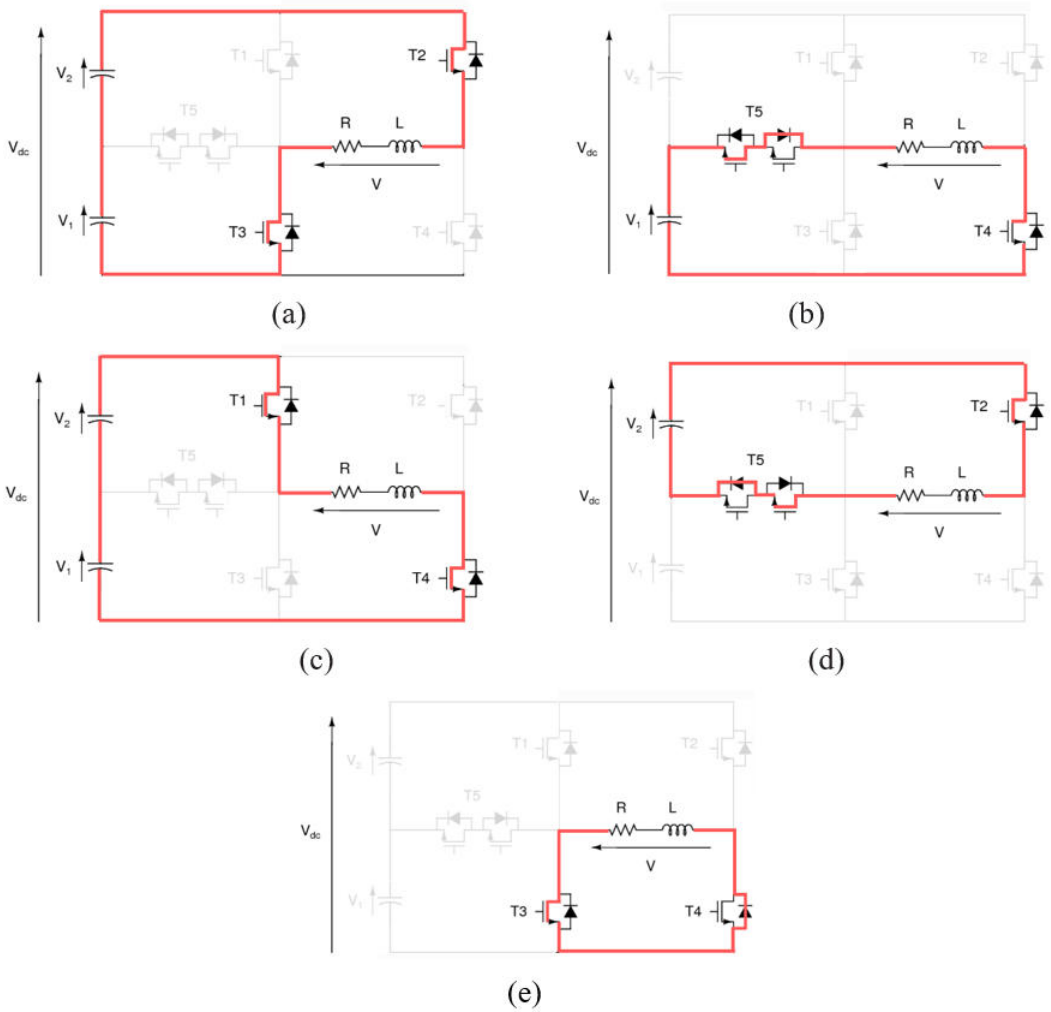


Figure 2.20 – Possible combination of T-type-MLI and their corresponding vectors.

$$i_l(k+1) = i_l(k) + \frac{T_s}{L}[v(k) - R.i_l(k)] \tag{2.18}$$

Table 2.8 – Voltage levels and switches states T_1,...,T_5

Voltages	T_1	T_2	T_3	T_4	T_5
$+ V_{dc}$	1	0	0	1	0
$+V_{dc}/2$	0	0	0	1	1
0	0	0	1	1	0
-$V_{dc}/2$	0	1	0	0	1
-V_{dc}	0	1	1	0	0

Table 2.9 – Voltage levels and variables S_a, S_b and S_c

Voltages	S_a	S_b	S_c
$+ V_{dc}$	2	1	0
$+V_{dc}/2$	1	1	0
0	2	0	0
-$V_{dc}/2$	1	0	1
-V_{dc}	2	0	1

Where: i_l (k+1): load current in the next sampling time, v(k): present load voltage, T_s: the sampling time. The output voltage of the inverter as a function of the switches' states is expressed as:

$$v = S_a.(\frac{V_{in}}{2}).(S_c - S_b) \tag{2.19}$$

$$V_{in} = V_{c1} + V_{c2} \tag{2.20}$$

S_a is the switching state of the auxiliary branch, whereas S_b and S_c are the switching states of the H-bridge arms. The variables S_a, S_b and S_c are expressed as follows:

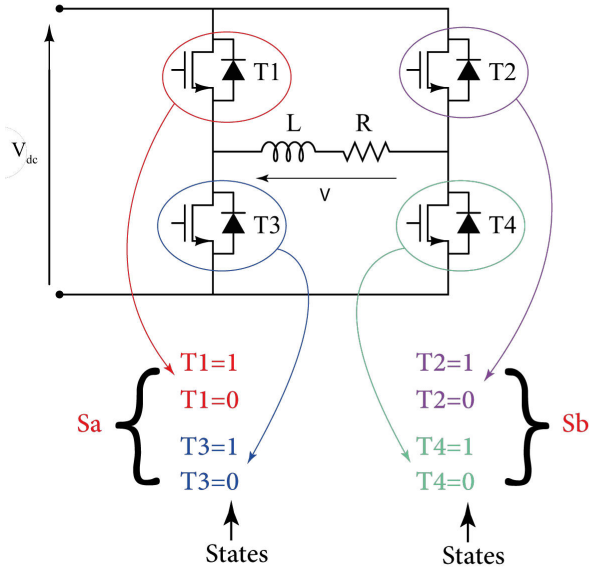
$$S_a = \begin{cases} 1 & \text{if } T_5{=}1 \\ 2 & \text{if } T_5{=}0 \end{cases} \tag{2.21}$$

$$S_b = \begin{cases} 1 & \text{if } T_1{=}1 \text{ and } T_3{=}0 \\ 0 & \text{if } T_1{=}0 \text{ and } T_3{=}0 \\ -1 & \text{if } T_1{=}0 \text{ and } T_3{=}1 \end{cases} \tag{2.22}$$

$$S_c = \begin{cases} 1 & \text{if } T_2{=}1 \text{ and } T_4{=}0 \\ 0 & \text{if } T_2{=}0 \text{ and } T_4{=}0 \\ -1 & \text{if } T_2{=}0 \text{ and } T_4{=}1 \end{cases} \tag{2.23}$$

These states are summarized in table 2.9.

Classic 2L-VSI



Voltages	T_1	T_2	T_3	T_4
$+V_{dc}$	1	0	0	1
0	0	0	1	1
0	1	1	0	0
$-V_{dc}$	0	1	1	0

The logical relationship (NOT) between every 2 switches **states (T1-T3, T2-T4)** help us to introduce 2 **variables** Sa and Sb for the 4 switches :

Sa=1 { T1=1, T3=0 } Sb=1 { T2=1, T4=0 }

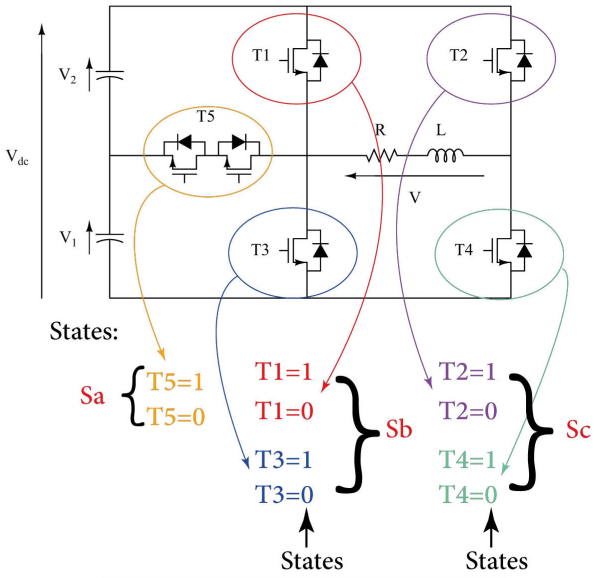
Sa=0 { T3=1, T1=0 } Sb=0 { T4=1, T2=0 }

Variable affected to states — Variable affected to states

Therefore:

$$V = V_{dc}(Sa - Sb)$$

Classic T-type



Voltages	T_1	T_2	T_3	T_4	T_5
$+V_{dc}$	1	0	0	1	0
$+V_{dc}/2$	0	0	0	1	1
0	0	0	1	1	0
$-V_{dc}/2$	0	1	0	0	1
$-V_{dc}$	0	1	1	0	0

The absence of logical relationship between the inverter switches **states** led us to introduce 3 **variables** Sa, Sb and Sc as follows:

$$Sa = \begin{cases} 1 \text{ if } & T5=1 \\ 2 \text{ if } & T5=0 \end{cases}$$

$$Sc = \begin{cases} 1 \text{ if } & T2=1 \ \& \ T4=0 \\ 0 \text{ if } & T2=0 \ \& \ T4=0 \\ -1 \text{ if } & T2=0 \ \& \ T4=1 \end{cases}$$

$$Sb = \begin{cases} 1 \text{ if } & T1=1 \ \& \ T3=0 \\ 0 \text{ if } & T1=0 \ \& \ T3=0 \\ -1 \text{ if } & T1=0 \ \& \ T3=1 \end{cases}$$

Variable affected to states

Therefore:

$$V = Sa.\left(\frac{V_{dc}}{2}\right).(Sc - Sb)$$

Figure 2.21 – T-type multilevel inverter modeling explanation scheme.

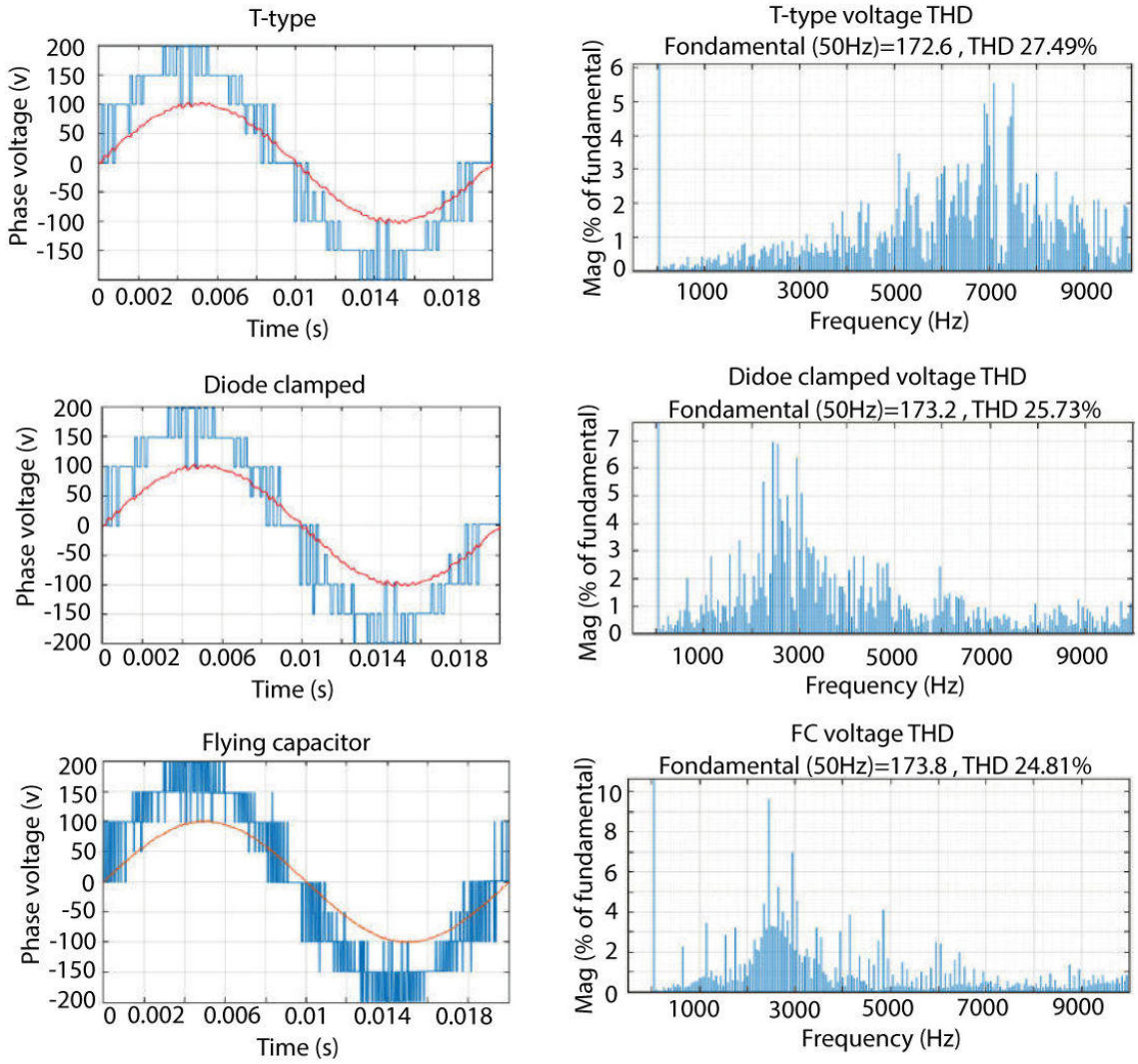


Figure 2.22 – Load current and voltage and voltage THD of various multilevel inverter types

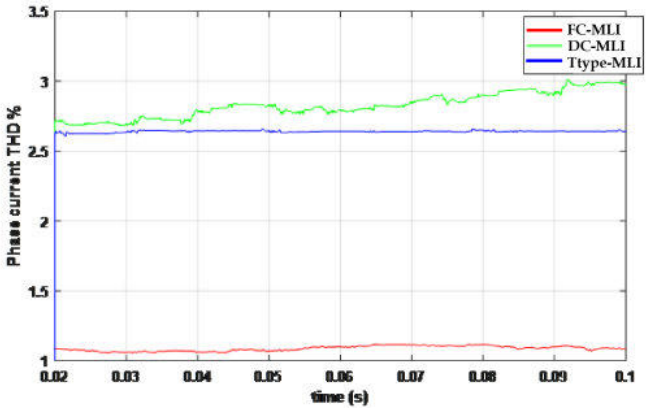


Figure 2.23 – Output current THD variation over time of T-type-MLI, DC-MLI and FC-MLI.

Table 2.10 – Comparison among various topologies according to various aspects, m: number of levels.

Topology	DC-MLI	FC-MLI	T-type-MLI	2L-VSI
Dc-link capacitors	(m-1)	(m-1)	(m-1)	1
balancing capacitors (per leg)	0	(m-1)· (m-2)/2	0	0
Clamping diodes (per leg)	(m-1)· (m-2)	0	0	0
Switches Ns	2(m-1) (leg)	2(m-1) (leg)	2(m-1) (leg)	2
Voltage THD % (phase)	25.73 %	27.49 %	24.81 %	109.74%
Current THD % (phase)	2.8 %	1.1 %	2.6 %	9%
Voltage unbalance	mean	high	Very small	small

From the current expression of the input capacitor, we can write:

$$\frac{d}{dt}\begin{bmatrix} V_{c1} \\ V_{c2} \end{bmatrix} = \frac{1}{C}\left(\begin{bmatrix} i_{c2} \\ i_{dc} \end{bmatrix} - \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}\right) \tag{2.24}$$

After discretization, we get:

$$\begin{bmatrix} V_{c1}(k+1) \\ V_{c2}(k+1) \end{bmatrix} = \begin{bmatrix} V_{c1}(k) \\ V_{c2}(k) \end{bmatrix} + \frac{T_s}{C}\left(\begin{bmatrix} i_{c2} \\ i_{dc} \end{bmatrix} - \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}\right) \tag{2.25}$$

The cost function is then:

$$g = \alpha|i_l^*(k+1) - i_l(k+1)| + \beta\sum_{p=1}^{4}|\frac{V_{dc}}{4} - V_{c_p}(k+1)|^2 \tag{2.26}$$

2.5 Results and discussion

The performance of the different topologies stated in section 2.2 namely: DC-MLI, FC-MLI, M-MLI, RS-MLI, Ttype-MLI, and PUC-MLI is investigated via simulation. Multiple criteria are taken into account in the evaluation like component count and the THD content of the output voltage and current. For a fair comparison, these multilevel inverters are simulated under similar conditions: same load, same sampling time T_s=1e-5s, R=17Ω, L=10mH, Vdc=300V)

Table 2.10 shows output THDs and expressions that help find the number of components such as DC-link input capacitors, floating capacitors, clamping diodes and switches. The results of these multilevel inverters are divided into 2 groups according to the similarity of their circuits: The load current and voltage THD of some of the inverters are shown in Figure 2.22, while Figure 2.24 refers to the rest.

The first group of Figure 2.22 contains the load current and voltage on the left-hand side and voltage THD on the right-hand side of T-type-MLI, DC-MLI and FC-MLI. Results showed that the FC-MLI output voltage has the lowest voltage THD with 24.8%, followed by the DC-MLI with a THD of about 25.7% then T-type-MLI with a value of 27.4%. Figure 2.24 exhibits the second group of results. The THD voltage showed the value of 39.3% for the M-MLI topology. Then, the RS-MLI one with 48.2%, and finally the PUC-MLI with 44%.

From table 2.10, we notice that the main drawback of classic multilevel inverters is the large number of clamping components. FC-MLI and DC-MLI suffer from large clamping components with a number of (m-1)(m-2)/2 capacitors and (m-1)·(m-2) diodes respectively. Based on the number of switches, all the multilevel inverters have the same number. The number of input capacitors (m-1) is the same among DC-MLI, FC-MLI and T-type-MLI. For the load current, FC-MLI showed the best value followed by the T-type MLI and then the DC-MLI with 2.8%.

Figure 2.23 and Figure 2.25 present the THD evolution of the output current over time. In Figure 2.23, FC-MLI presents the lowest total harmonic distortion. DC-MLI has the highest THD level with 3.7%. T-type-MLI recorded a lower current THD with a 3.6%. [11]. In Figure 2.25, the THD curve presents considerable fluctuations. These fluctuations are due to the charge and discharge of capacitors of the input side. Therefore, by considering the mean value of each curve, The lowest THD value is recorded by the RS-MLI with 3.03%, then the M-MLIs and PU-MLI with an identical result of 3.08%.

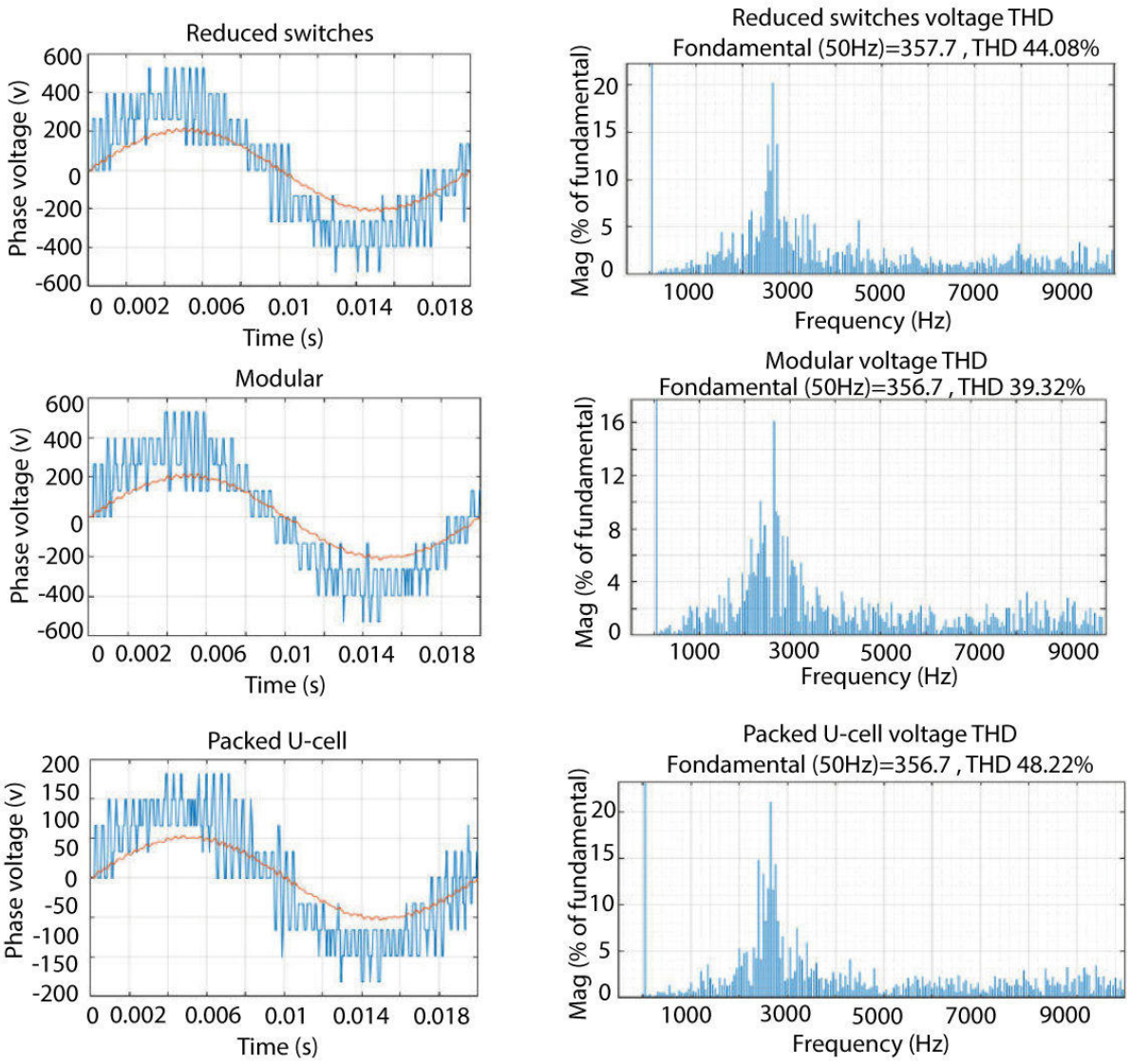


Figure 2.24 – Load current and voltage and their voltage THD of various multilevel inverter types

2.6 Conclusion

In this chapter, we started by walking through various multilevel topologies by analysing their different characteristics. Firstly, basic multilevel inverters such as NPC, FC and CC were investigated, and then multiple emerging topologies like RS, packed E-cell and T-type multilevel inverters were also thoroughly studied. In section 2.3 We exhibited various control techniques with their types. The first family is Pulse Width Modulation(PWM) which was developed to suit multilevel inverters. By modifying the reference and carrier, several improvements have emerged to come with better performance for instance: third

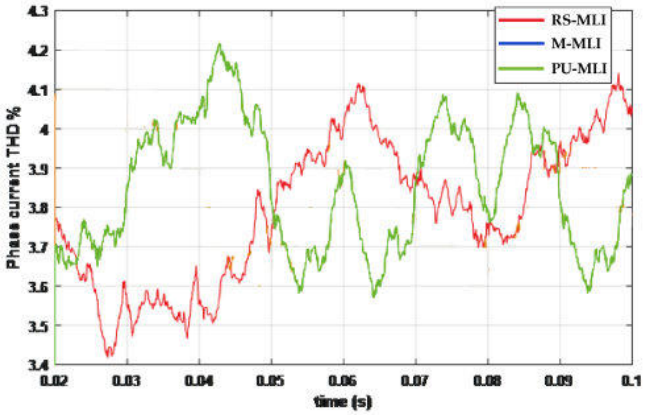


Figure 2.25 – Current THD variation over time among RS-MLI, CC-MLI and PUC-MLI.

harmonic injection PWM (THPWM), space vector PWM (SVPWM), PD, POD, APOD, PS. Also, Model Predictive Control MPC emerged during the two last decades as a powerful tool for the control of power electronics and drives. This technique covers a large family of techniques from which FS-MPC is the most used in the literature nowadays. This later technique is explained in detail, where it was applied to a 3-level T-type multilevel inverter as an example. The same technique is used to control a variety of multilevel inverters such as PUC-MLI, M-MLI, RS-MLI and PUC-MLI under the same simulation conditions. Results showed that RS-MLI has a better load current THD face to the other structures (M-MLI, RS-MLI and PUC-MLI). Furthermore, regarding the voltage quality, T-type-MLI showed the best quality with 24.81%. In principle, it was found that RS-MLI with PUC-MLI and T-type have the most appealing qualities.

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Chapter 3

Photovoltaic grid-connected system: Healthy and Faulty cases

3.1 Introduction

As we saw in Chapter 2 , PV systems are constituted of several parts: PV panels, DC-DC converters, DC-AC inverters and a grid for grid-connected PV systems or a passive load if it is an off-grid system. In this section, we tackle a brief review of each of these parts.

DC-AC converters were rapidly developed in the last decades, specifically, Multilevel inverters that paved the way in industry. Their structure was improved in terms of the circuit topology and its connection with the other parts within the system. Multilevel inverters have the ability to operate in medium voltage applications (medium voltage grid-connected systems based on renewable energies, medium voltage variable speed drive systems, HVDC systems, ... [1] [2]. multilevel inverters are considered as the development of traditional two-level inverters 2L-VSI which cannot operate in medium voltage ranges [3]. The main role of multilevel inverters is to synthesize a staircase waveform, usually called a pseudo-sinusoidal waveform consisting of several levels generated from input capacitors. As a result, the harmonics of the output currents and voltages are remarkably reduced, approaching zero as the voltage levels are increased. In addition, we benefit from less electromagnetic interference and a reduced common mode voltage. Moreover, multilevel inverters are capable of operating at lower switching frequencies without trouble. [4].

We distinguish three traditional families of multilevel inverters, namely: a) neutral point clamped converter (NPC) or diode clamped multilevel converter (DC-MLI), b) flying capacitor converter(FC-MLI), and c) cascaded H-bridge converter or modular M-MLI.

This later is characterized by its modular structure which suits very well PV applications. Each PV panel is connected to a single H-bridge, which improves the efficiency of the overall system, particularly in the case of shading or mismatches [5]. Despite that it only generates two levels, connecting multiple H-bridges allows dividing the input voltages among these converters, thus permitting the operation at higher power. This, however, makes the global converter costly and complicated for the control [6].

The FC-MLI topology requires a grand number of capacitors. The presence of such a number requires a complex control and extra control circuit due to the voltage imbalance which causes bad output waveforms [7]. Regarding the DC-MLI topology, this type of multilevel inverter demands an excessive number of diodes as the voltage level increases, which causes more losses [8]. Variants of the previous topology have recently emerged such as hybrid multilevel converters (also called active neutral point clamped converter ANPC, hybrid H-bridge converter, hybrid ANPC converter,...) and also the T-type power converter [9] [10–15].

Other emerging topologies are presented in the literature, such as the T-type converter. T-type multilevel inverters exhibit various advantages such as reduced conduction losses, relatively low switching, high efficiency, and fault tolerance options. The topology of this T-type converter is composed of a full H-bridge and an auxiliary circuit of bidirectional switch combination. The shape of this converter gives it the possibility of four-quadrant functioning [16], [17].

Recently, Finite Set-Model Predictive Control (FS-MPC) gained a lot of attention in research. It appeared as an attractive control method giving a powerful approach to the control of power converters. FS-MPC become very mature showing a brilliant performance, for instance: its fast transient response, dispensing off linear controllers and modulators (PWM or SVM). Its modulation technique is radically different compared to PWM, very simple, and hardware-friendly with standard microprocessors, particularly with the fast advancement of processors. The approach is established starting from the fact that a power converter can generate a finite number of possible switching states. The mathematical model of the system predicts the behaviour of the variables that correspond to each switching state. Then, with a designed cost function, the selection of the appropriate switching state is evaluated for the predicted values at each sampling time. Then, the optimal state which minimizes the cost function is selected to be applied at the next sampling time [18].

In general, the photovoltaic grid-connected system (PVGCS) scheme is constituted of two stages of converters: an MPPT chopper, and a converter connected in cascade with a two-level voltage source inverter. For the control circuit, each converter is controlled independently. In this chapter, as a first contribution, the study proposes an optimized

control of the two converters instead of controlling them separately. The advantage of this technique is that it avoids the use of two control circuits, and therefore, considerably reduces the hardware implementation.

Table 3.1 – Some fault-tolerant techniques based on the proposed control in literature

Fault-tolerant techniques	contribution	complexity	limitations	Additional hardware
Carrier-Based PWM [22]	- SPWM-based control strategy - Modifying the modulation when fault occurs -Fours simultaneous fault-tolerance -Maintaining the capacitor voltages balanced	Division of the inverter into sub-inverter	Open-circuit fault only	No
Switching Mode Operation based on FS-MPC [23]	-FS-MPC-based control strategy -One fault treated that is open-circuit. -Maintaining the capacitor voltages balanced	Possible additional Hardware for fault detection – a costly solution	Open-circuit fault only	Yes
The present paper	-FS-MPC-based control strategy -Two types of faults studied short-circuit and Open-circuit -Two simultaneous fault-tolerance -Maintaining the capacitor voltages balanced	Uses hardware of normal control for detection	/	No

All along the operation of PV systems, power electronics components burn from 3-5 times [19]. This rate is greater than any component in the rest of the PV systems. Unfortunately, the repair of these components causes the interruption of power production. This interruption is considered as a significant problem in PV systems, let alone when it is placed in remote zones. It also causes a strong reduction in the capacity factor of the plant. The solution in industry is simply to replace the broken components. In scientific papers, failures in power electronics are an important subject that requires more attention, for example, introducing novel methods dealing with these failures from either a "diagnostic" perspective or from a "reliability" point of view [20], [21], [22] [22]. There is very little research dealing with this aspect by just introducing additional components or circuits.

In [23], researchers present a fault-tolerant method applied to an NPC by sub-dividing

the converter into sub-inverters and using a modified modulating technique based on PWM. This method is limited to the case of open-circuit faults in switches. In [24], the researchers presented a modified FS-MPC method. The type of inverter used is a Packed E-Cell inverter. Likewise, the method of the previous research deals only with open-circuit failure in switches without treating the short-circuited fault. In addition to that, the authors didn't indicate if they have added additional hardware elements or not. Table 3.1 covers briefly a comparison among the aforementioned works.

A second contribution in this chapter is a proposed control technique which is a modified IFS-MPC. This technique deals with certain failure scenarios such as short-circuit of input capacitor and open-circuit in a switch. in this second study, we embark on an additional case which is a short-circuit failure. Furthermore, a combined case when a short-circuit failure and an open-circuit fault are triggered at the same time is also treated. One of the important pros of this proposed method is preventing the interruption of power generation when a sudden fault occurs, which means that this method perfectly suites systems placed in difficult hard-to-reach sites, for instance, offshores renewable systems and space systems. Throughout the simulation results of the two faulty scenarios, we will maintain the continuity of the service of the system thanks to the proposed control algorithm which does not include any additional hardware and instead uses the already existing voltage sensors in the DC-link side (balancing sensors) as well as the load side (load sensor). [25]

The chapter is organized into three sections as follows: Section I presents an introduction, Section II concerns the normal healthy operation of the grid-tied PV system. Section III is dedicated to the faulty operation of the grid-tied PV system. In part 1 of Section II, we show the advantage of the hybrid predictive-incremental conductance MPPT algorithm over the classic incremental conductance technique. Meanwhile, in the second part of the section, the global system using the T-type inverter, is controlled by means of the proposed integrated control IFS-MPC. Section 3 shows the simulation results for the two studied scenarios for failure conditions and are presented under modified IFS-MPC to sense and reject the faulty cases, without the need for adding any extra hardware components. The results are commented on and interpreted. Finally, a conclusion is stated.

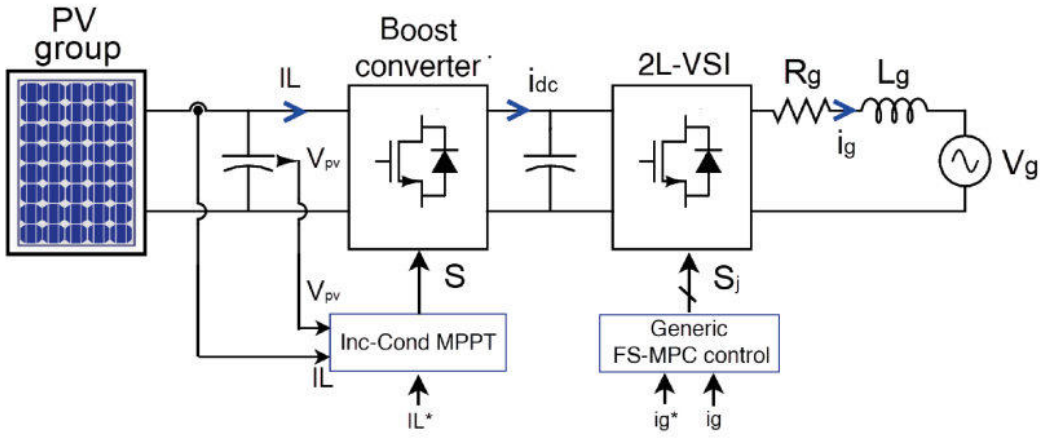

Figure 3.1 – General PVGCS scheme with FS-MPC control technique.

3.2 Healthy operation of grid-connected PV system

3.2.1 Hybrid predictive incremental-conductance MPPT

The scheme of the general photovoltaic grid-connected system (PVGCS) is depicted in Figure 3.1. In general, it consists of two stages, that is: a boost converter connected to a two-level voltage source inverter (2L-VSI) in a cascaded manner. Each converter has its own control system independently. The boost/buck stage usually uses classic tracking methods such as Perturb and Observe (PO), Incremental conductance (Inc-Cond), Hill Climbing (HC), and many other advanced algorithms as stated beforehand. Meanwhile, the 2^{nd} stage converts the DC energy to AC with the driving of different control strategies, such as FS-MPC control. Figure 3.2 shows the boost converter in its conventional configuration. It increases the input voltage V_{pv} up to higher value V_{load} through a special switching pattern of the controllable switches.

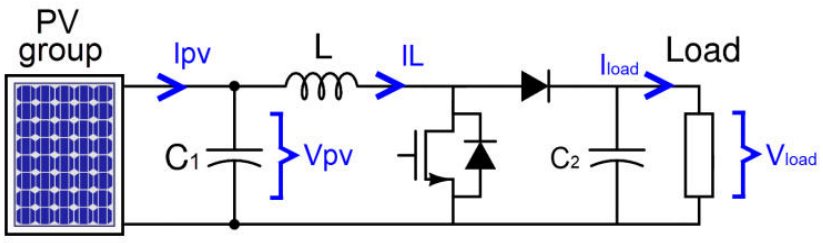

Figure 3.2 – The circuit of a conventional boost converter.

We can write the voltage at the output of the boost converter as:

$$V_{load} = \frac{1}{(1-D)} V_{pv} \tag{3.1}$$

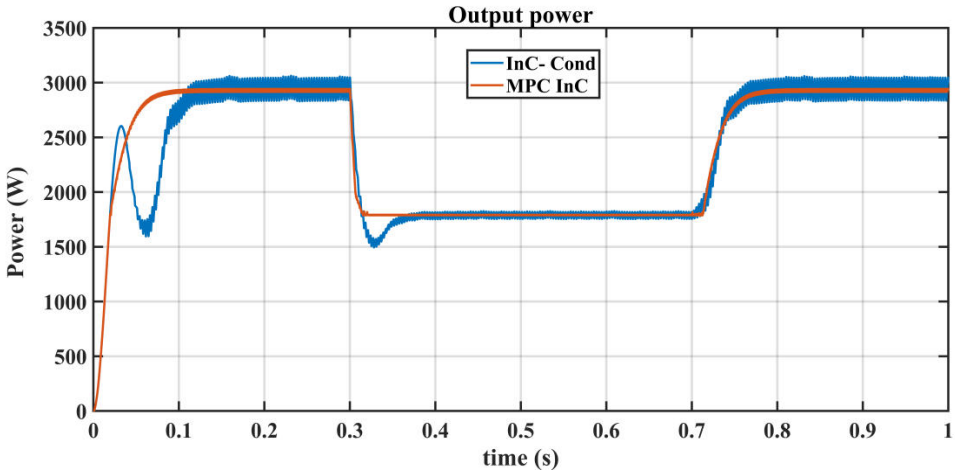

Figure 3.3 – Output power of the MPC Inc-Cond versus classic Inc-Cond in case of a sudden change of irradiance.

Where: D is the duty cycle, V_{load} is the load voltage and V_{pv} is the PV voltage at the input. The boost chopper contains two states: ON and OFF, therefore it can be modelled as: If the switch is ON then (S=1):

$$i_L(k+1) = i_L(k) + V_{pv}(k)\frac{T_s}{L} \tag{3.2}$$

$$V_{pv}(k+1) = V_{pv}(k) + (I_{pv}(k) - i_L(k))\frac{T_s}{C_1} \tag{3.3}$$

If the switch is OFF then (S=0):

$$i_L(k+1) = i_L(k) + (V_{pv}(k) - V_{load}(k))\frac{T_s}{L} \tag{3.4}$$

$$V_{pv}(k+1) = V_{pv}(k) + I_{pv}(k) - I_L(k))\frac{T_s}{C_1} \tag{3.5}$$

From equations 3.2, 3.3, 3.4 and 3.5 we can write the average model of the boost converter:

$$i_L(k+1) = i_L(k) + (V_{pv}(k) - (1-S)\mathrm{V}_{load}(k))\frac{T_s}{L} \tag{3.6}$$

$$V_{pv}(k+1) = V_{pv}(k) + (I_{pv}(k) - i_L(k))\frac{T_s}{C_1} \tag{3.7}$$

Throughout the literature over the last three decades [26] [27], the Inc-Cond algorithm technique is considered as the most popular MPPT technique among classical methods.

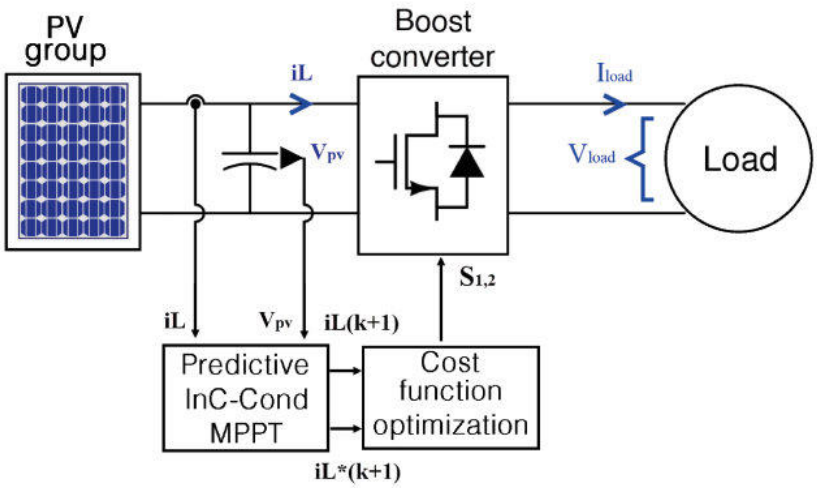

Figure 3.4 – Hybrid Inc-Cond Predictive MPPT technique scheme.

Nonetheless, it remains suffering from many drawbacks, namely the slow transient state, oscillations at the MPP during the steady state, and possible instability of the output due to the derivative di_{pv}/dv_{pv} on which the algorithm is based, inability to handle shading and mismatch conditions which shows in its poor performance. In addition, this technique faces difficulties at low levels of irradiance. To overcome these limitations, (Figure 3.4) proposes a hybrid Predictive Inc-Cond control which has more ability to better track the MPP for both transient and steady states even at low irradiance conditions.

Figure 3.6 depicts the flowchart of the Hybrid Inc-Cond Predictive MPPT algorithm applied to a boost converter. In this algorithm, the classic Inc-Cond technique generates the reference value of the coil current [28]. After that, this later becomes an input to the predictive cost function g which minimizes the current error and chooses the most suitable switching state of the boost converter, so that it will be applied at the next sampling time. To visually clarify the performance of the two MPPT controls: Hybrid Inc-Cond Predictive MPPT and the classical one were examined for both transient and steady state. Figure 3.3 depicts the power variations under a quick change in the irradiance level according to the profile [1000 – 700 – 1000] W/m^2. From the curves, it is clear that the hybrid MPC-Inc-Cond control outperformed the Inc-Cond since the MPP is tracked more accurately and more efficiently for both states.

3.2.2 Grid-tied PV system

3.2.2.1 Multilevel T-type inverter

The T-type inverter is considered as an advanced multilevel inverter topology thanks to the various advantages it enjoys over the classic 2L-VSI, such as operation under voltages

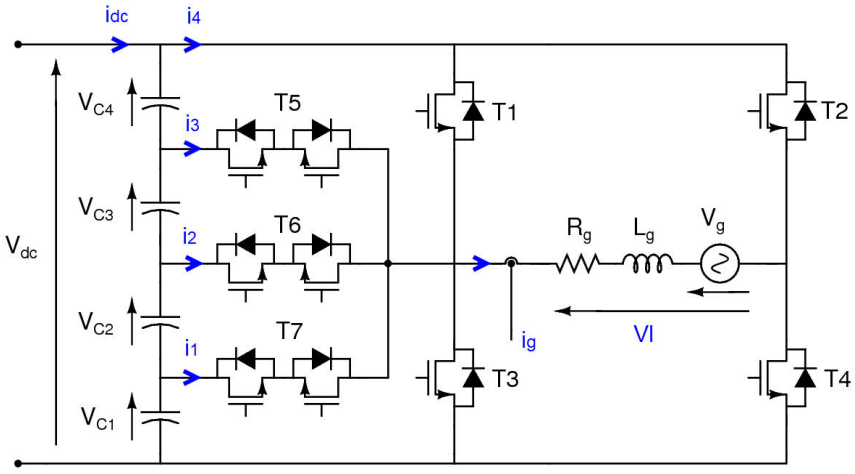

Figure 3.5 – Power circuit of the 5-level T-type inverter.

Table 3.2 – Voltage levels of 7-level T-type inverter with their corresponding states

Output voltage Vl	T1	T2	T3	T4	T5	T6	T7
+ v	1	0	0	1	0	0	0
+3v/4	0	0	0	1	1	0	0
+2v/4	0	0	0	1	0	1	0
+v/4	0	0	0	1	0	0	1
0	1	1	0	0	0	0	0
0	0	0	1	1	0	0	0
-v/4	0	1	0	0	1	0	0
-2v/4	0	1	0	0	0	1	0
-3v/4	0	1	0	0	0	0	1
-v	0	1	1	0	0	0	0

that exceed the withstanding of the switching devices, lower common-mode voltages, light voltage changes (dv/dt). Five-level T-type inverters are composed of an H-bridge and a circuit of bidirectional controllable switches as shown in Figure 3.5. This later circuit allows the operation at voltage levels higher than those of the conventional 2L-VSI depicted in Figure 3.1. The DC-link capacitors are supposed to deliver a voltage of Vdc/4 for each one where (Vc1= Vc2 = Vc3 =Vc4=Vdc/4) [29].

Table 3.2 presents the various voltage levels with their respective states of the 7 switches: T1-. . .-T7. From the table, we can see that there are no redundant voltages except for the zero vector.

The different states of the 5-level T-type inverter are illustrated in the different 7 subfigures of Figure 3.7 for a healthy operation without faults.

3.2.2.2 Mathematical model of FS-MPC

The output voltage is given by the following equation 3.8:

$$v(t) = R_g.i_g(t) + L_g\frac{di_g}{dt} + v_g(t) \tag{3.8}$$

Where: i_g: grid current, v_g: grid voltage, v: output voltage, R_g,L_g: filter resistor, inductance respectively, T_s: sampling time.

$$i_g(k+1) = i_g(k) + \frac{T_s}{L_g}[v(k) - v_g(k) - R_g.i_g(k)] \tag{3.9}$$

Where: i_g: grid current, v_g: grid voltage,v: output voltage, R_g,L_g: filter resistor, inductance respectively, T_s: sampling time.

The voltage at the output of the inverter, also the DC-link voltage equation is expressed as follows in equations 3.10, and 3.11 :

$$v = S_a.(\frac{V_{dc}}{4}).(S_b - S_c) \tag{3.10}$$

$$V_{dc} = V_{c1} + V_{c2} + V_{c3} + V_{c4} \tag{3.11}$$

S_a is the switching state of the auxiliary circuit, while, S_b and S_c are considered the switching states of the H-bridge arms. The equations 3.12, 3.13 and 3.14 that define S_a, S_b and S_c are expressed as follows:

$$S_a = \begin{cases} 1 & \text{if } T_7{=}1 \text{ and } T_5{=}T_6{=}0 \\ 2 & \text{if } T_6{=}1 \text{ and } T_5{=}T_7{=}0 \\ 3 & \text{if } T_5{=}1 \text{ and } T_6{=}T_7{=}0 \\ 4 & \text{if } T_5{=}T_6{=}T_7{=}0 \end{cases} \tag{3.12}$$

$$S_b = \begin{cases} 1 & \text{if } T_1{=}1 \text{ and } T_3{=}0 \\ 0 & \text{if } T_1{=}1 \text{ and } T_3{=}1 \end{cases} \tag{3.13}$$

$$S_c = \begin{cases} 1 & \text{if } T_2{=}1 \text{ and } T_4{=}0 \\ 0 & \text{if } T_2{=}0 \text{ and } T_4{=}1 \end{cases} \tag{3.14}$$

The previous states of equation 3.12, 3.13 and 3.14 are summarized in the table 3.3.

The current passing through a capacitor can be expressed by the following equations:

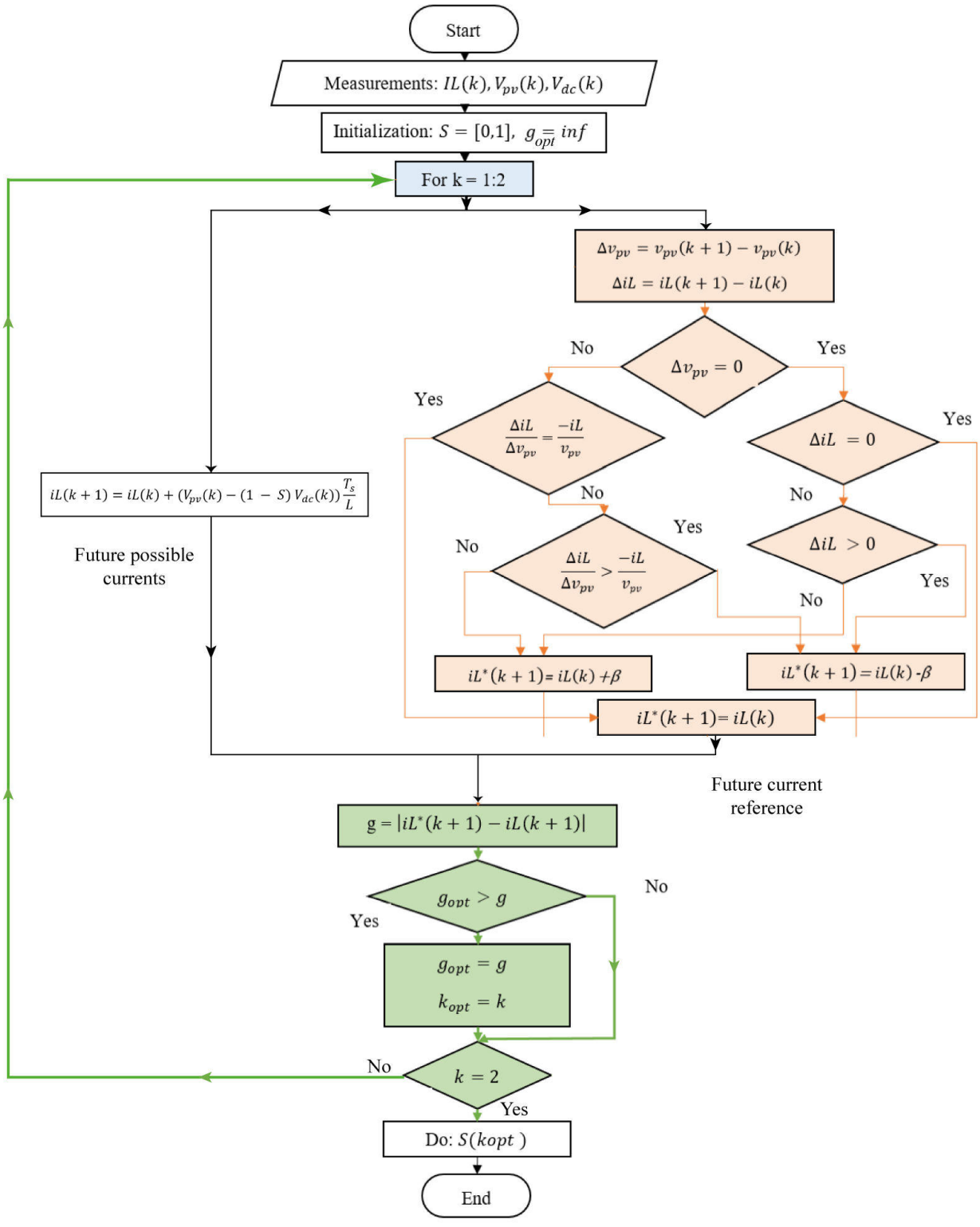

Figure 3.6 – Flowchart of the hybrid Predictive Inc-Cond technique.

$$\frac{d}{dt}\begin{bmatrix} V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \end{bmatrix} = \frac{1}{C}\left(\begin{bmatrix} i_{c2} \\ i_{c3} \\ i_{c4} \\ i_{dc} \end{bmatrix} - \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix}\right) \tag{3.15}$$

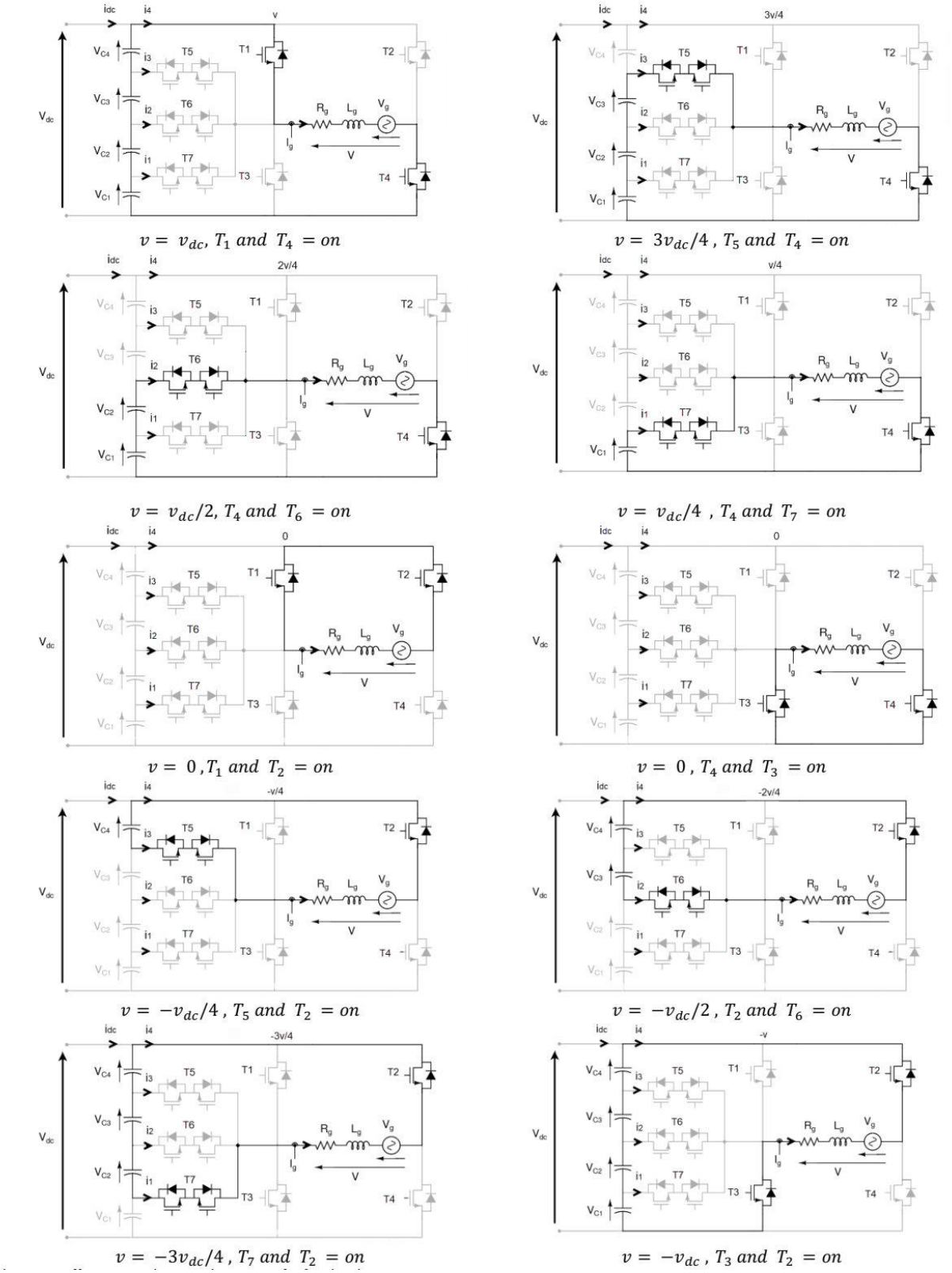

Figure 3.7 – Different switching combinations of a five-level T-Type converter.

Table 3.3 – Possible voltage levels as a function of variables S_a, S_b, S_c.

States	S_a	S_b	S_c
$+V_{dc}$	4	1	0
$+(3V_{dc})/4$	3	1	0
$+(2V_{dc})/4$	2	1	0
$+V_{dc}/4$	1	1	0
0	4	0	0
$-V_{dc}/4$	1	0	1
$-(2V_{dc})/4$	2	0	1
$-(3V_{dc})/4$	3	0	1
$-V_{dc}$	4	0	1

Using Euler discretization, we get:

$$\begin{bmatrix} V_{c1}(k+1) \\ V_{c2}(k+1) \\ V_{c3}(k+1) \\ V_{c4}(k+1) \end{bmatrix} = \begin{bmatrix} V_{c1}(k) \\ V_{c2}(k) \\ V_{c3}(k) \\ V_{c4}(k) \end{bmatrix} + \frac{T_s}{C} \left(\begin{bmatrix} i_{c2} \\ i_{c3} \\ i_{c4} \\ i_{dc} \end{bmatrix} - \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \right) \tag{3.16}$$

The basic structure of PV grid-tied systems has usually 2 independent control systems, as shown in Figure 3.1. The first control circuit deals with the MPPT assured by a boost/buck converter, while the 2nd circuit takes care of the desired performances on the grid. By using FS-MPC technique, control algorithm 1 has one cost function g1 which deals with the PV current, thus, g1 is minimized for 2 switching states of the chopper. Control algorithm 2 can include several terms depending on the desired performance, such as grid current error and capacitor voltage balancing. The cost function g2 is thus minimized for the 9 non-redundant switching states of the T-type inverter. the main contribution of this 1st part is to present an integrated topology by using only one control algorithm having integrated cost function g that groups all the objectives cited above. Hence, the two power converters are considered to be seen by the control circuit as an indirect matrix converter with 18 switching states as shown in Figure 3.8.

The results by simulation of the 2 topologies in Figures 3.1 and 3.8 are compared to show the performance of each structure. The cost function of the MPPT control is:

$$g_1 = |(i_L)^*(k+1) - i_L(k+1)| \tag{3.17}$$

The cost function at the inverter side is as follows:

$$g_2 = \beta |i_g^*(k+1) - i_g(k+1)| + \gamma \sum_{p=1}^{4} |\frac{V_{dc}}{4} - V_{c_p}(k+1)|^2 \tag{3.18}$$

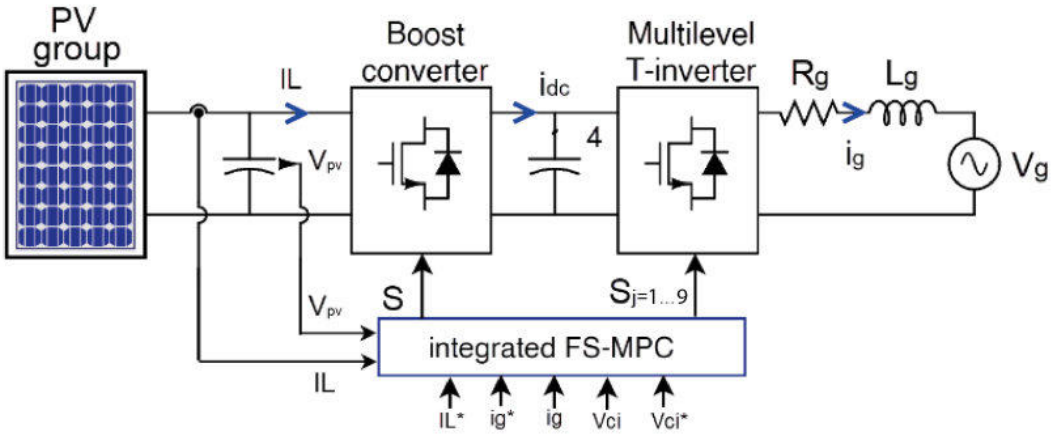

Figure 3.8 – The proposed Integrated FS-MPC for the control of PV-GCS.

The expression of the integrated cost function g is as follows:

$$g = \alpha|(i_L)^*(k+1) - i_L(k+1)| + \beta|i_g^*(k+1) - i_g(k+1)| + \gamma \sum_{p=1}^{4} |\frac{V_{dc}}{4} - V_{c_p}(k+1)|^2 \quad (3.19)$$

According to the desired performance, additional objectives can be added for example switching numbers:

$$g = \alpha|(i_L)^*(k+1) - i_L(k+1)| + \beta|i_g^*(k+1) - i_g(k+1)| + \gamma \sum_{p=1}^{4} |\frac{V_{dc}}{4} - V_{c_p}(k+1)|^2 + \mu N_{sw} \quad (3.20)$$

Where α, β, γ and μ are weighting factors. [30]. The number of switchings of the IGBTs is given by:

$$N_{sw} = \sum_{n=1}^{11} |S_n(k) - S_n(k-1)| \quad (3.21)$$

Where: $S_n(k)$ is the present state of a switch T_i. $S_n(k-1)$ is the state of the same switch T_i in the previous sampling time.

3.3 Faulty operation of grid-connected PV system

Grid-connected PV systems are more likely to be subjected to various faults on the inverter level such as DC bus capacitors or power switches [24], [31–33]. To maintain the healthy functioning of the PVGCS system and preserve the grid-connection standards after faulty conditions, we propose a modified control algorithm design called M-IFS-

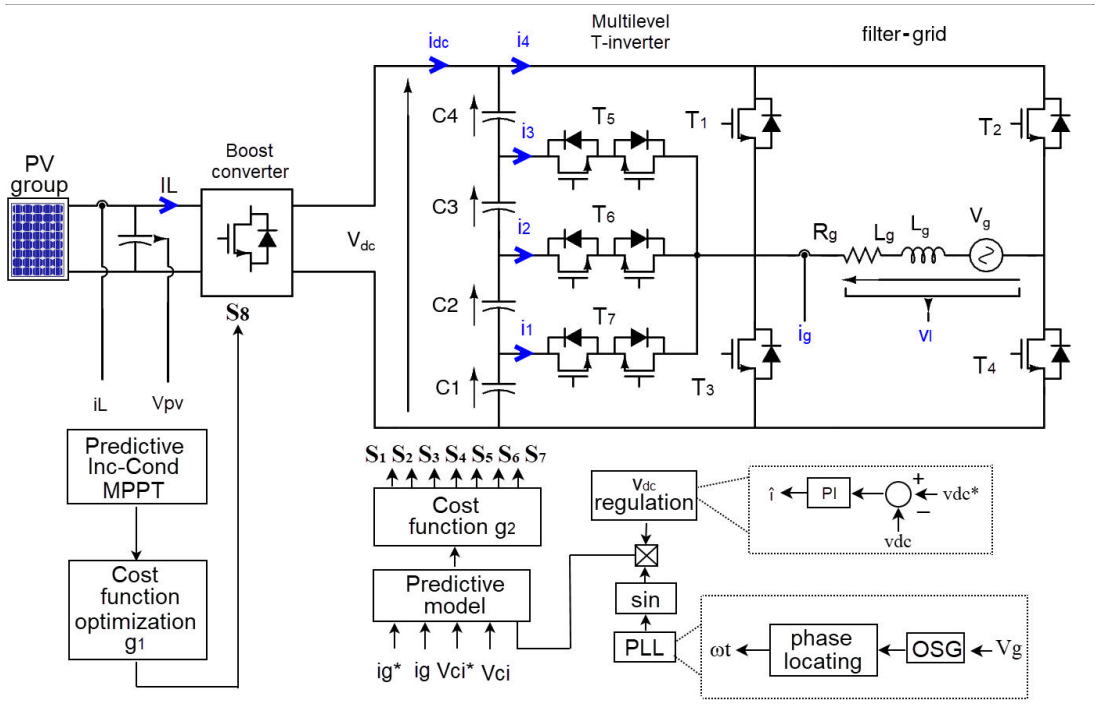

Figure 3.9 – The control scheme of a generic PVGCS by using the FS-MPC technique.

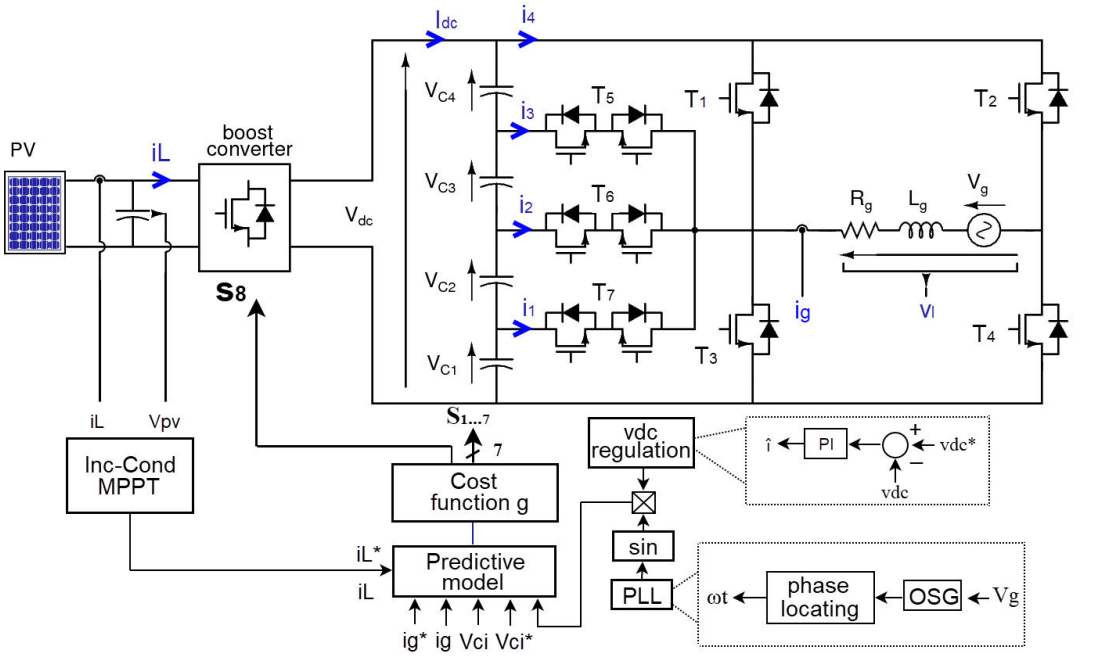

Figure 3.10 – The Control scheme of the FS-MPC applied to the proposed PVGCS.

MPC. Two scenarios are examined, in the first one, a DC-link capacitor fails and a switch breaks down in the second one. This algorithm allows the inverter to shift easily between five and four levels of operation modes without the need to intervene on the power circuit

level.

3.3.1 Scenario 1: Short-circuit of the capacitor

Generally, a DC-link is constituted at least of one capacitor or more. Usually, the selection of these capacitors is imposed by the electrical system. This selection is not only based on electric parameter sizing. In fact, It also depends on various other factors, for example, exposure to extreme conditions (ambient temperature, humidity, etc.), also, constraints on power rate applications. Therefore, depending on the type of capacitor, we find 3 modes of failure: short circuit failure, open circuit failure, and wear-out failure. Short circuit failure is the most common mode of failure in DC-link capacitors, so, it is considered in the present study [34] [35] [19] [36]. In the current study, we examine short-circuit failure. the detection of this failure is by means of the already existing voltage sensors devoted to voltage balancing. Voltage drops in ideal short-circuits is equal to zero. Hence, this concept is coded as a condition in the proposed control algorithm, which detects whether it is a healthy or failure mode and decides to work in a five-level or four-level mode. In this first scenario, we suppose that one of the DC link capacitors (C_2) gets a short-circuit at instant 0.3s, this means that v_{c2} =0. The operation of the T-Type inverter is then modified, hence, in the model of the inverter the variable S_{a1}' of the auxiliary branch becomes as follows:

$$S'_{a1} = \begin{cases} 1 & \text{if } T_6{=}1 \text{ and } T_5{=}T_6{=}0 \\ 2 & \text{if } T_5{=}1 \text{ and } T_6{=}T_7{=}0 \\ 3 & \text{if } T_5{=}T_6{=}0 \end{cases} \tag{3.22}$$

$$S_b = \begin{cases} 1 & \text{if } T_1{=}1 \text{ and } T_3{=}0 \\ 0 & \text{if } T_1{=}0 \text{ and } T_3{=}1 \end{cases} \tag{3.23}$$

$$S_c = \begin{cases} 1 & \text{if } T_2{=}1 \text{ and } T_4{=}0 \\ 0 & \text{if } T_2{=}0 \text{ and } T_4{=}1 \end{cases} \tag{3.24}$$

The output voltage of the inverter becomes:

$$v_l = S'_{a1}(\frac{V_{dc}}{3})(S_b - S_c) \tag{3.25}$$

Eventually, the voltage in the DC-link is given by:

$$V_{dc} = V_{c1} + V_{c3} + V_{c4} \tag{3.26}$$

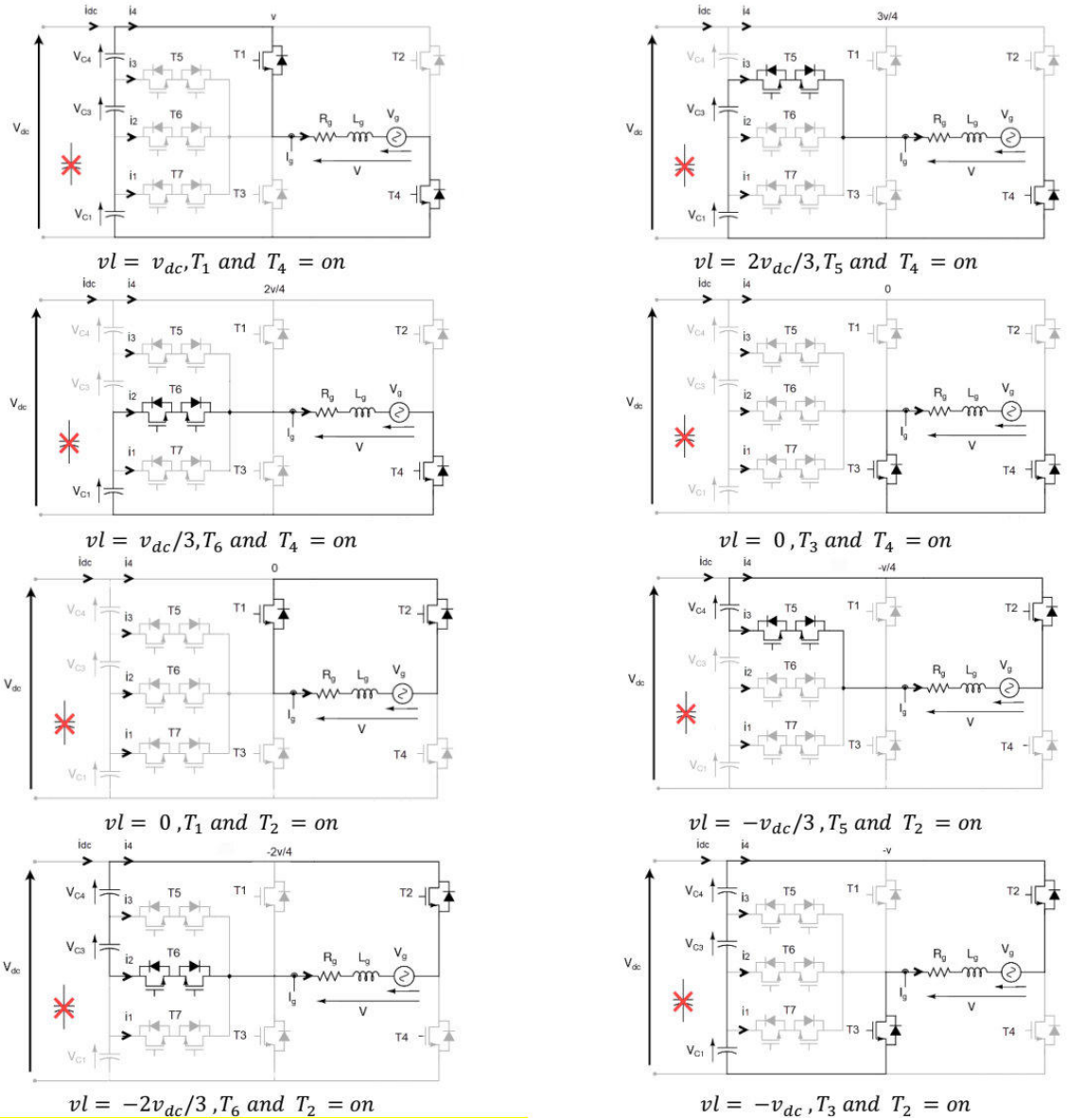

Figure 3.11 – Circuit phases in a case of a short-circuit in capacitor C_2 of the DC-link.

The possible non-redundant operating vectors of the inverter are now eight (7) states instead of 9. They are summarized in Figure 3.11.

Instead of 5 output levels, they become only 4 now (Vdc, 2Vdc/3, Vdc/3, 0) and are given by table 3.4.

Table 3.4 – Different output voltage levels for scenario 1.

States	S_a1'	S_b	S_c
$+V_{dc}$	3	1	0
$+(2V_{dc})/3$	2	1	0
$+V_{dc}/3$	1	1	0
0	3	0	0
$-V_{dc}/3$	1	0	1
$-(2V_{dc})/3$	2	0	1
$-V_{dc}$	3	0	1

3.3.2 Scenario 2: Open-circuit of the switch

Generally, for power switches, we find 2 modes of failure: short-circuit and open-circuit [37]. In the current study, the faulty mode is the open-circuit failure. The voltage sensor of the load is used to detect the absence/presence of a certain voltage level; therefore, the open-circuit failure is sensed by the absence of a particular voltage level, in this case, v_{c2}. When the control technique detects the faulty state, it segregates the broken switch and changes the operation from 5-level to 4-level operation. Furthermore, Let's examine a complicated case when two faults occur simultaneously. That is a short circuit of capacitor C_2 which occurs at 0.2 s (scenario 1), followed after that by a breakdown of switch T6 at instant 0.6 s resulting in a combined fault.

Considering these assumptions, the inverter will have to switch from five to four-level mode. The operation of the T-Type inverter is then modified, so the logic variable S_{a2}' of the auxiliary circuit becomes as follows:

$$S'_{a2} = \begin{cases} 1 & \text{if } T_7{=}1 \text{ and } T_5{=}T_5{=}0 \\ 2 & \text{if } T_5{=}1 \text{ and } T_6{=}T_7{=}0 \\ 3 & \text{if } T_5{=}T_7{=}0 \end{cases} \tag{3.27}$$

$$S_b = \begin{cases} 1 & \text{if } T_1{=}1 \text{ and } T_3{=}0 \\ 0 & \text{if } T_1{=}0 \text{ and } T_3{=}1 \end{cases} \tag{3.28}$$

$$S_c = \begin{cases} 1 & \text{if } T_2{=}1 \text{ and } T_4{=}0 \\ 0 & \text{if } T_2{=}0 \text{ and } T_4{=}1 \end{cases} \tag{3.29}$$

The output voltage of the inverter becomes:

$$v_l = (S_{a2})' \frac{V_{dc}}{3}(S_b - S_c) \tag{3.30}$$

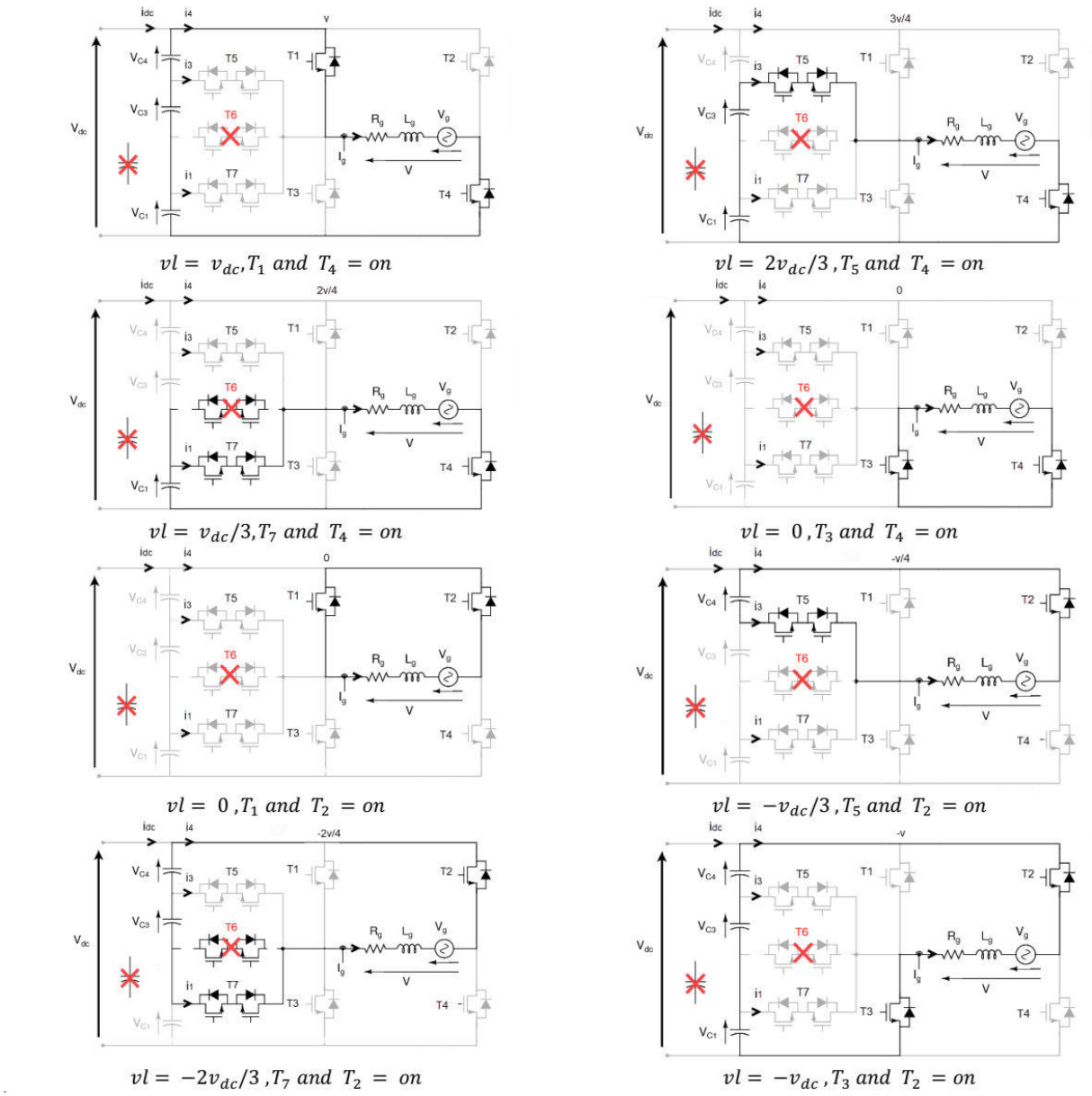

Figure 3.12 – Operating phases of the converter under combined faults.

The output voltages are now four (4) (Vdc, $\frac{2Vdc}{3}$, $\frac{Vdc}{3}$, 0) instead of five (5). The possible operating voltages of the inverter are seven (7) and are depicted in Figure 3.12 Eventually, the DC-link voltage is expressed by:

$$V_{dc} = V_{c1} + V_{c3} + V_{c4} \tag{3.31}$$

3.4 Results and discussion

A series of simulations using Matlab-Simulink software have been conducted in order to show the advantage of the proposed Integrated control technique IFS-MPC over the classic control technique FS-MPC. For the simulation we used the same parameters for simulation and for power circuit parameters as listed in the following table 3.5(under the same conditions of simulation).

Table 3.5 – Parameters of the on-grid PV system Parameter Value

Parameter	Value
PV	300 W
Group PV (52)	3 kW
current at MPP	8.1 A
voltage at MPP	36.7 V
Capacitor boost input C	3 F
Capacitor DC-link $C_1, 2, 3, 4$	4.5 mF
Inductor L	25 mH
Filter inductor L_g	3.5 mH
Internal inductor resistor R_g	0.1
Grid RMS voltage V_g	220 V
Sampling time T_s	30s

Figure 3.13 depicts the curves of output current, output voltage and THD for both separated strategy on the right side and integrated control strategy IFS-MPC on the left side. All the curves are simulated for 3 profiles of irradiation [1000-700-1000] W/m2. For the grid current i_g and DC-link voltage regulation V_{dc} the results are close to their reference for both steady state and transient one. For the grid current THD and output voltage vl, we observe similar results, whether in a transient or steady state. We deduce that integrating the cost functions does not negatively affect the performance of the system.

In order to guarantee the proper functioning of the PVGCS in case of the two types of faults, a modified algorithm is designed called M-IFS-MPC. The principal idea of the proposed algorithm is to keep the same voltage of the DC-link value for both healthy and faulty modes. When a fault is detected in the inverter, the reference voltage value is updated for each DC-link capacitor to keep the global DC-link voltage constant at the new value such that: for the healthy mode, V_{ci}^{*}=Vdc/4, when a capacitor in the converter is short-circuited, the new reference for each capacitor voltage becomes now V_{ci}^{*}=Vdc/3. This switched control mode will preserve the well-functioning of the system without degradation of the system power quality such as low THD and unity power factor operation. The proposed control algorithm is depicted in Figure 3.15, where the overall

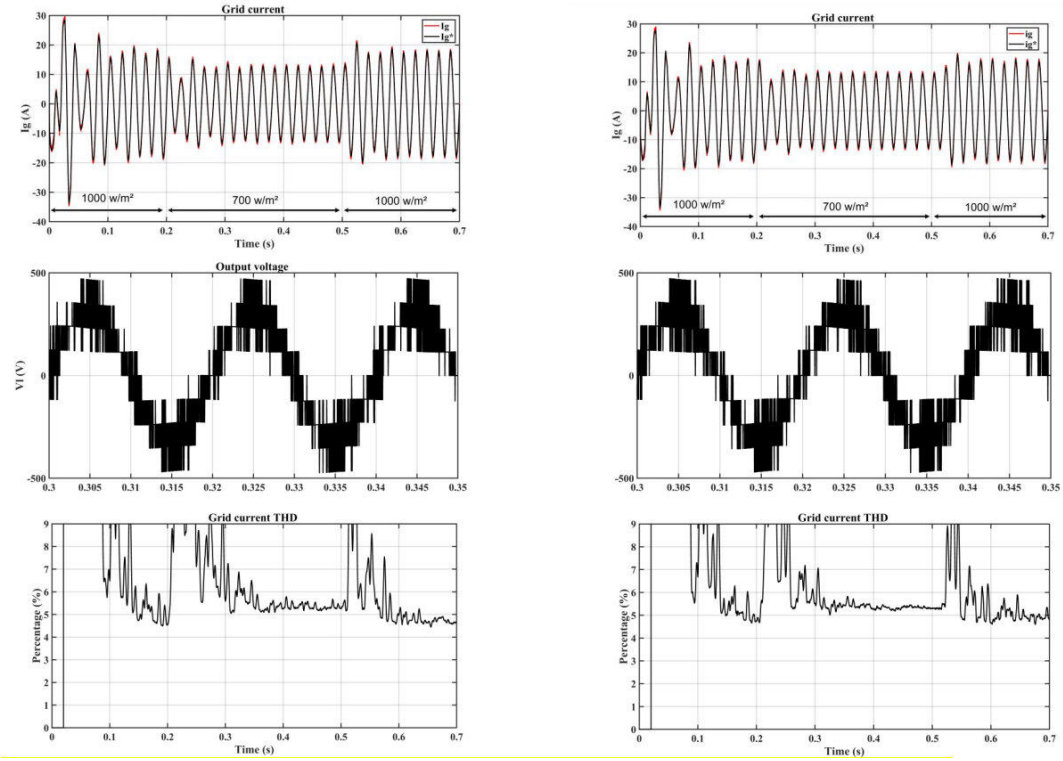

Figure 3.13 – Simulation results for integrated and separated FS-MPC (DC-link regulation, grid output and current voltage with current THD).

cost function is minimized for 14 switching states instead of the 18 we have in the healthy case.

Figure 3.15 depicts the flowchart of M-FS-MPC. it takes into consideration the healthy state as well as the failed one. If the system is in a healthy state the algorithm thus runs a 5-level FS-MPC control. At each instant k, the sizes stated under the label "start" $V_{dc}(k)$,$i_L(k)$,$V_{pv}(k)$,$i_g(k)$ are measured. besides, at each instant k, the algorithm tests whether there is a fault in all capacitors of the DC-link and the auxiliary switches. These tests are carried out without adding external circuits or components. In fact, it uses the DC-link capacitors' balancing sensors and the output voltage sensor. When a failure of one DC-link capacitor is detected (capacitor 2), the voltage reference for each capacitor is updated to $v_{dc}/3$. The MPPT generates the reference current iL in addition to the grid current i_g and the reference voltage capacitors'. Eventually, when the voltage vector is selected, the algorithm takes a dead time of less than one period to carry out a second test to decisively decide whether the auxiliary switches are correctly working or not. If one of the auxiliary switches (switch 6 in scenario 2) is burned down, the control algorithm selects another combination of switches to produce the same lost voltage level. Basically, the overall proposed control algorithm is simple, it just needs voltage sensors of each capacitor and the current load sensor. These sensors are used to sense and locate the

failure then the algorithm intervenes to make a decision about the system's functioning.

Scenario 1 Figure 3.14 displays a set of simulation results of the PVGCS in the case when one of the capacitors is short-circuited at instant 0.3s. The control operates in a healthy mode in the range [0- 0.3] s with 5-level operation. In this range, the 4 capacitors' voltages are balanced, and thus the system works well at unity power factor. At t=0.3 s, we assume that the 2nd capacitor C2 is short-circuited (Vc2 =0). this causes a transient state in the DC-link voltage. As we can see, the modified control algorithm M-IFS-MPC is activated and will update the voltage reference and generate a new reference voltage for the rest healthy capacitors. With the global DC-link voltage equal 440V, so, V_{ci}^{*}= 440/3 V instead of 440/4 V. During that transient state, the inverter output voltage shifts from 5-level to 4-level mode without affecting the power quality injected into the grid due to the fact that the system goes back to the healthy state before the failure by working at unity power factor, as shown by the zoomed area.

Scenario 2 This scenario is depicted in the set of simulation results that appears in Figure 3.16, we assume that the previous short-circuit of scenario 1 in the capacitor C2 but this time occurs at 0.2s, followed by a failure in the auxiliary circuit switch T6 at 0.6s. The functioning profile of the considered system can then be divided into 3 zones. During the period [0 - 0.2] s, the operation of the system is healthy where the inverter generates five levels at unity power factor with 5% THD of the grid current. In the interval [0.2 – 0.6] s, the inverter moves from five-level to four-level mode without affecting the quality of the output power of the grid. At moment t=0.6s, a combined failure occurs when switch T6 breaks down. Then, the inverter begins to lose almost all the voltage levels as highlighted with the red arrow in the interval [0.6 – 0.62] s of Figure 3.17 before redeeming them at instant t=0.62s thanks to switch T7 which comes into service by replacing T6 after one period as shown in Figure 3.16. After 0.62 s, the inverter retrieves the four voltage levels without affecting the power quality injected into the grid.

To illustrate the influence of the M-IFS-MPC in the failure functioning of the PVGCS with correspondence with the grid THD standards, Figure 3.18 illustrates the THD of the grid current for scenarios 1 and 2. At first, in the healthy zone, the THD is about 5% in the steady state, after the first failure (capacitor short-circuited) it becomes around 7.5% without correction. when M-IFS-MPC was activated, the THD is decreased to its initial value of 5%. When the combined faults occur (at 0.6 s), the THD jumps again to 9.5%. However, this later value is diminished again to its initial value of 5% when the M-IFS-MPC algorithm is activated.

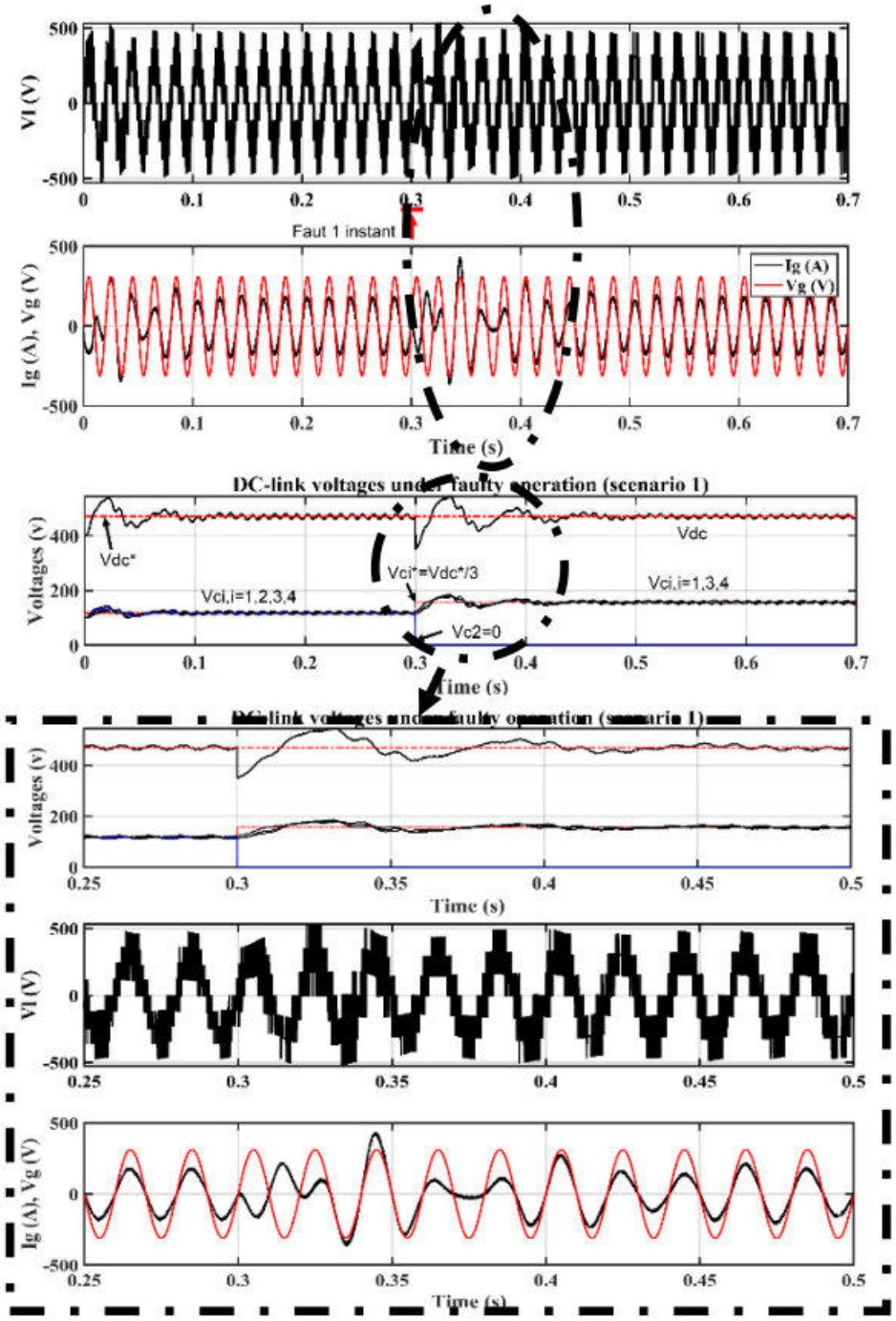

Figure 3.14 – Results for scenario 1(DC-link capacitor short-circuited): Output voltage, voltage grid current, DC-link voltages with their zoom.

3.5 Conclusion

In Chapter 3, we started with an introduction where we introduced a brief background on the parts of PV systems. After that, we presented two contributions for PVGCSs. The first one is an optimized predictive control called IFS-MPC which has the merit of

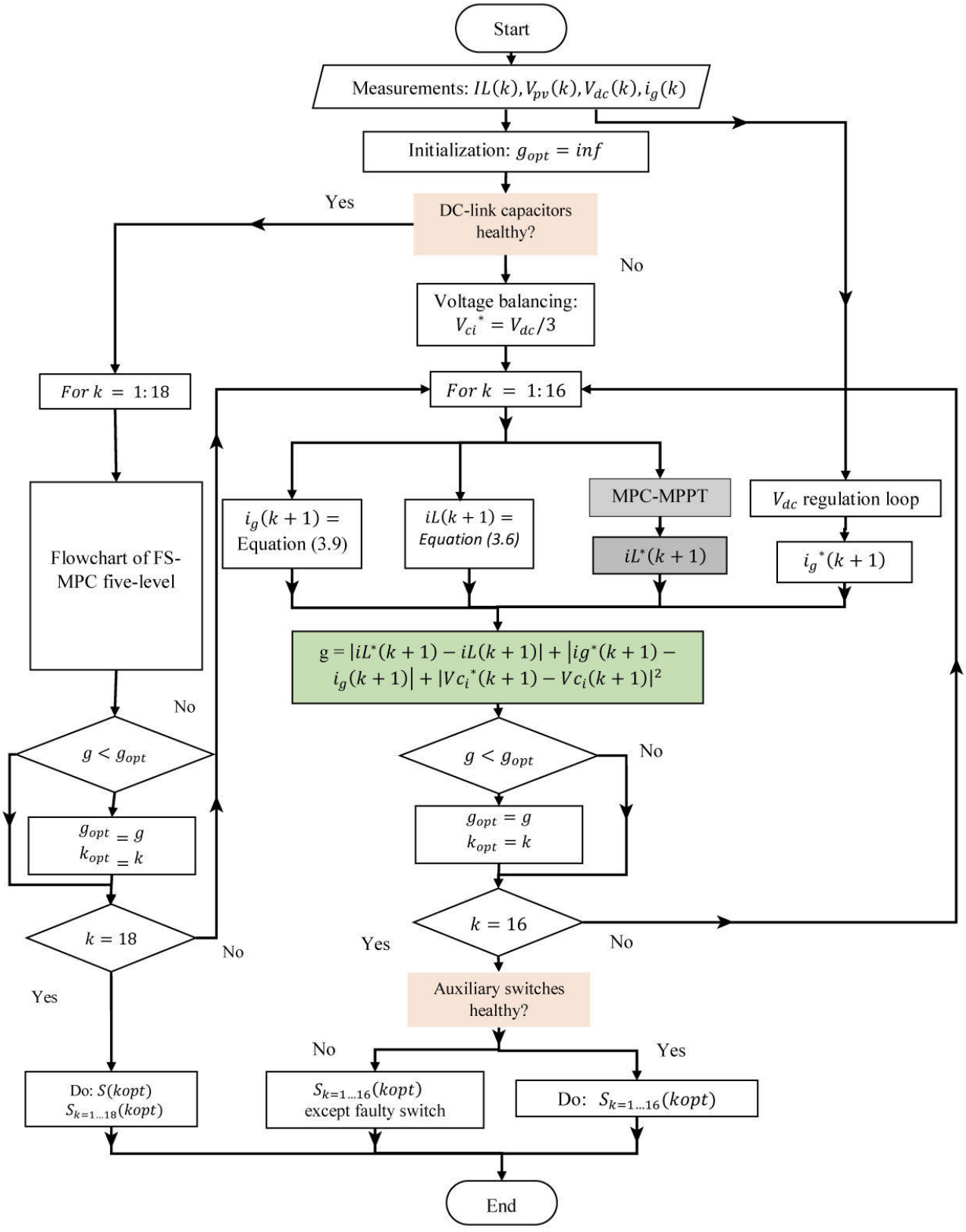

Figure 3.15 – Flowchart of the proposed M-IFS-MPC for the faulty mode of the power converter.

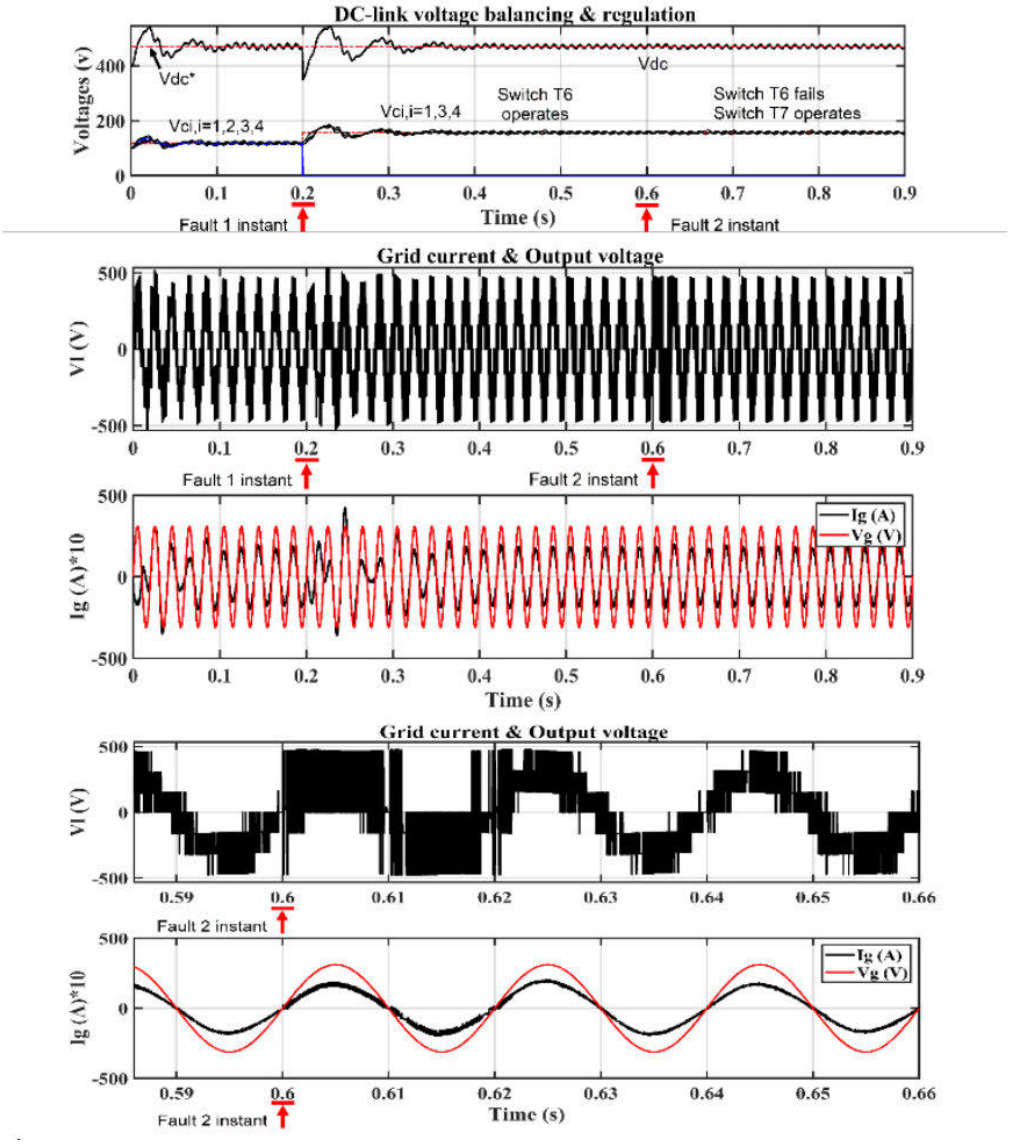

Figure 3.16 – Simulation results for scenario 2: DC-link voltages, Output inverter voltage, voltage, and grid current with their zoom.

controlling two cascaded connected converters as an indirect matrix converter. The T-type inverter and the boost chopper are controlled at the same time by using one cost function instead of using two and controlling them separately, as a result, the control circuit of the system is greatly reduced. The performance of the IFS-MPC technique is studied via simulation. It showed that we can achieve high dynamic and static performances as in the case when each converter is controlled separately, without influencing the quality of the power of the grid. The second part of the chapter dealt with the extension of the proposed control design to systems operating under converter faults. To cope with the various failures that are possible to occur in the inverter, such as a short circuit of the capacitors

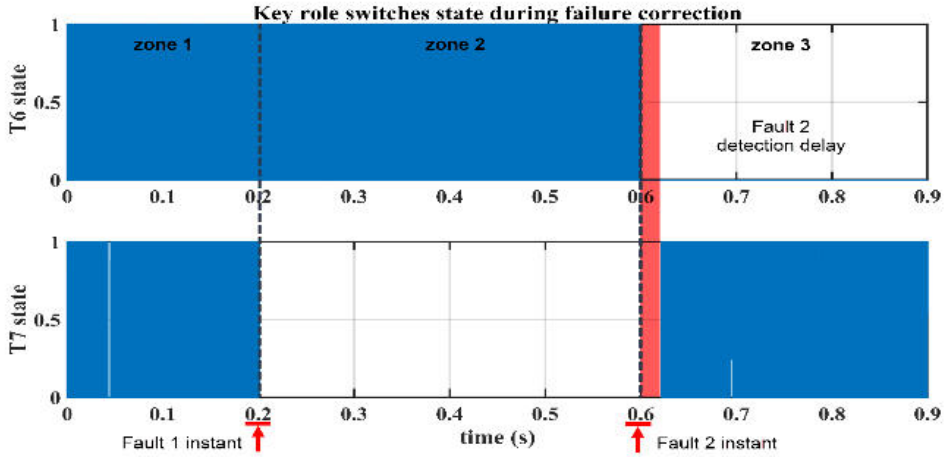

Figure 3.17 – Key role switches state during failure correction.

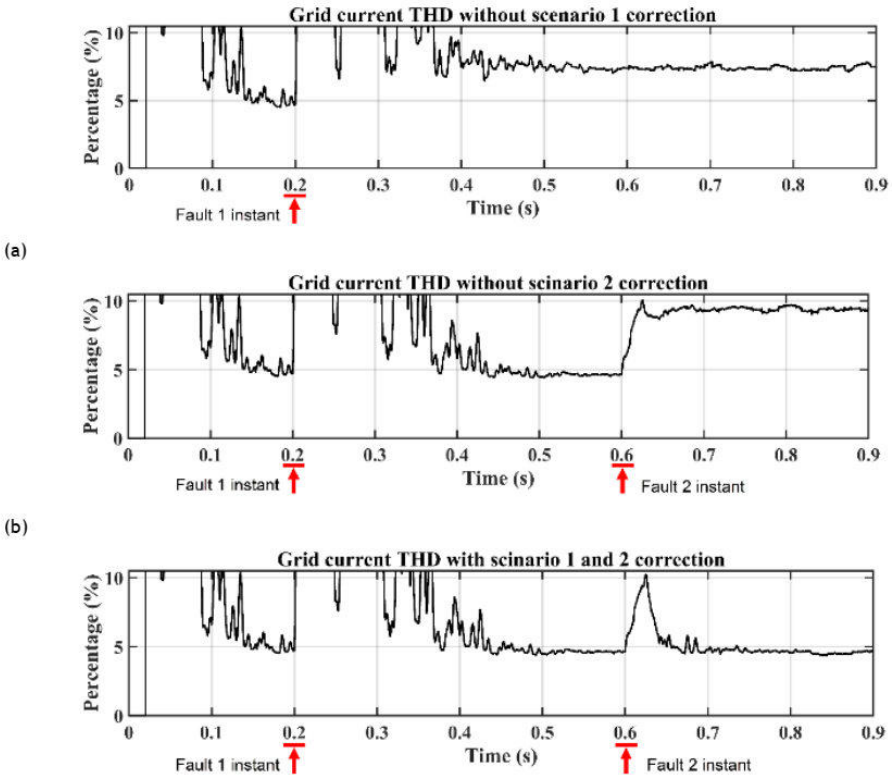

Figure 3.18 – The impact of M-IFS-MPC on the THD of grid current: (a). without scenario one (1) correction. (b). without scenario two (2) correction. c. with M-IFS-MPC correction

in the DC-link and a failure of the switches, a modified M-IFS-MPC is developed and examined. The three (3) terms of the cost function are selected meticulously to match the requirements of the PVGCS. The proposed design for both healthy and faulty systems allows moving at any instant from a five-level to a four-level mode operation by a proper selection of the voltages in the auxiliary DC-link without a negative effect on the power

quality of the grid. Also, without the involvement of hardware circuits. The results of the performance of the M-IFS-MPC are excellent for both static and dynamic regimes of the controlled system. The IFS-MPC proved that it is reliable to be used efficiently under faulty conditions of power converters. These conclusions are to be further confirmed through a practical realization in future works.

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Chapter 4

A wings T-type (WT-type) multilevel inverter with reduced cost and enhanced efficiency

4.1 Introduction

As mentioned in the previous chapter, there are mainly three families of multilevel converters: a) neutral point clamped converter (NPC), b) flying capacitor converter (FC) and c) cascaded H-bridge inverter [1] [2]. Flying capacitor topology requires a large number of capacitors and thus voltage balancing which raises the complexity of the control circuit [3]. The H-bridge inverter topology uses its modular nature to reduce the input voltages by dividing it among the set of modules connected in series. This characteristic on the other hand makes the converter costly. In the NPC topology, the number of clamped diodes becomes excessive the more the voltage levels are high. This causes more losses and thus lower efficiency. To cope with all these cons, researchers proposed novel multilevel circuit variants [4] [5].

The present chapter aims to propose a multilevel inverter topology called Wings T-type (WT-type). This topology is derived from the classical T-type multilevel inverter and can be easily expanded to generate higher levels. The optimization process is presented for a five-level T-type multilevel inverter. After that, a detailed analysis of the characteristics of the studied multilevel inverter is carried out and then controlled using the FS-MPC technique for evaluation. The results of simulation and practical experimentation are interpreted and compared to those of the classical inverter in terms of power losses, cost, power quality, and thermal stress.

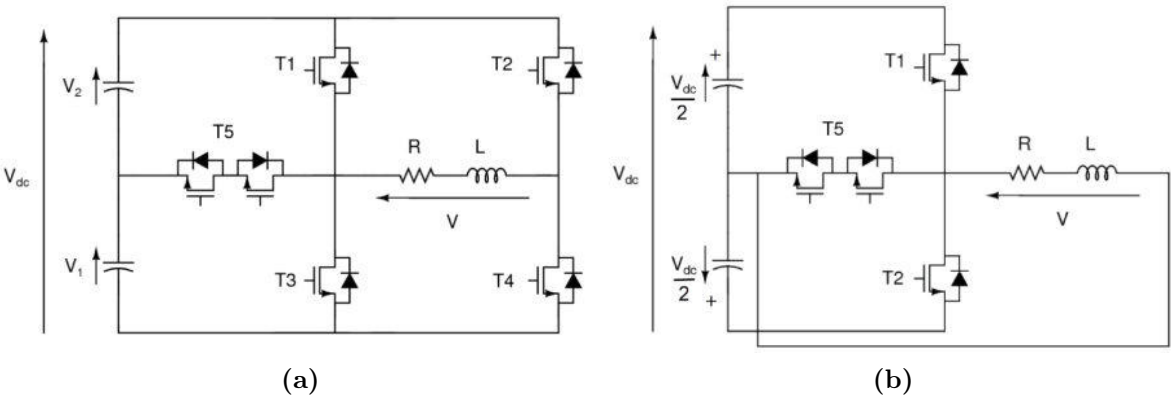


Figure 4.1 – Modes of connection of T-type (a) full bridge based (b) half-bridge based.

4.2 State of the art of T-type multilevel inverters

A lot of efforts to resolve the problems of conventional topologies were developed. As a result, the T-type converter is among the first circuits proposed to enhance the characteristics of the NPC MLI. It enjoys the advantages of low conduction losses, high efficiency, and a lower number of components [6]. It is composed of an auxiliary circuit connected to either an H-bridge as shown in Figure 4.1a, or connected to a half-bridge inverter as in Figure 4.1b. The full H-bridge generates upper levels of ±vdc value [7]. while half-bridge-based T-type can only generate upper levels of ±vdc/2. The auxiliary circuit in both cases gives the levels ±vdc/2 in the H-bridge-based one or the level 0 in the half-bridge-based one. Table 4.1 and table 4.2, detail the output voltages and their corresponding switching states.

By comparing the T-type converter to traditional NPC and FC MLIs, the NPC uses diodes to clamp input sub-voltages to the arm of switches. This later requires a large number of switches as well as diodes for the generation of the required levels. Meanwhile, in FC MLIs, additional passive components (capacitors) are used as clamping elements to help generate the inverter's sub-voltages. The T-type converter optimizes the clamping mechanism in the previous multilevel inverters. T-type converter introduces an auxiliary circuit with bidirectional switches to produce various steps of voltage. In addition, every bidirectional switch is controlled using only one gate signal, hence, we get a simple design of the control circuit. Furthermore, for an equal output level, the number of switches is significantly reduced .

To develop the characteristics of the T-type multilevel inverter such as the number of components, efficiency, thermal distribution, cost, ... researchers developed considerable efforts to produce new topologies based on the two basic circuits presented in Figure 4.1:

Table 4.1 – Switching states and their corresponding voltages of inverter in Figure 4.1a

T1	T2	T3	T4	T5	Vl
1	0	0	1	0	+Vdc
0	0	0	1	1	+Vdc/2
0	0	1	1	0	0
0	1	0	0	1	-Vdc/2
0	0	0	0	0	- Vdc

Table 4.2 – Switching states and their corresponding voltages of inverter in Figure 4.1b

T1	T2	T5	Vl
1	0	0	+Vdc/2
0	0	1	0
0	1	0	-Vdc/2

In [8] (2014) researchers stated various drawbacks of the NPC multilevel inverter. During its operation, the current has to circulate through a lot of semiconductor components which causes higher conduction losses. In addition, it induces high parasite inductance which results in overshoot voltages at switching-off transitions which results in lower efficiency. Therefore, the clamping circuit of the NPC is transformed into a circuit in the form of "T", hence, the current's path becomes shorter as shown in the 2014 circuit on the timescale. In the improved circuit, conduction losses are remarkably reduced.

In [9] (2016), the authors proposed a topology of inverters named Nested T-type inverter (NT-type) as shown on this Figure. This topology is a hybrid structure that combines classic T-type with Flying capacitor multilevel inverter. This inverter consists of fewer components compared to the NPC and FC MLIs, which improves the overall efficiency. The main drawback of this topology remains the number of auxiliary capacitors which raises the complexity of the inverter at higher voltage levels.

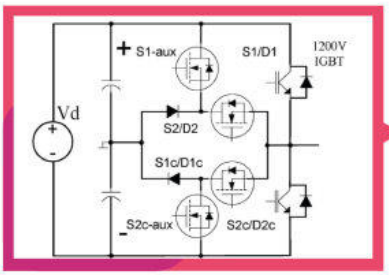
In [10] (2017-1) researchers proposed an asymmetrical inverter topology as presented in the Figure. This inverter is capable of producing output voltages starting from 17 levels. To increase output levels we connect multiple modules in series. The inverter contains a low number of switches which reduces the volume of the cooling system and the PCB volume. On the other hand, the asymmetrical nature of the inverter implies the use of switches with high voltage rates which raises the overall cost.

in [11] (2017-2), the authors propose an asymmetrical topology that consists of two parts: an H-bridge and a half-bridge-based T-type inverter as depicted in Figure. The first part contains a single capacitor that creates the voltage level 'E' and the second part consists of 2 capacitors for levels 2E and -2E as shown on the circuit. The authors examined the characteristics of the proposed inverter using SPWM and SVM control techniques. Results showed that with SPWM control, capacitors are maintained balanced only if the modulation index is under 0.82. For SVM, the modulation index threshold can be extended to 1.15 without having unbalanced capacitors. For the device count,

this topology contains lower switches than the classical inverters for the same number of levels. However, since the inverter is asymmetrical, this means that components must endure higher reverse blocking voltages which relatively increase their cost.

In [12] (2018-1), a single-phase modified T-type inverter is studied. The circuit is designed by a series of switches connected in an interfered manner forming arms "a" and "b" as shown in the Figure. The first arm contains an auxiliary circuit with bidirectional switches $\overline{Q_{a1}}$ and Q_{a2} connected drain to drain. Meanwhile, the auxiliary circuit of the second arm "b" contains bidirectional switches $\overline{Q_{b1}}$ and Q_{b2} connected source to source. The studied topology includes 2 capacitors (i.e. produces 3 levels). The switches count of the presented topology is 8, whereas, the classical T-type inverter contains only 6. This means that the proposed circuit is not cost-efficient. On the other hand, the complementary operation of each two switches reduces the complexity of the control circuit by having fewer drivers.

In [13] (2018-2), the authors propose a topology characterized by crossed-connected switches circuit as shown in Figure. It is composed of two half-bridge-based T-type inverters placed on both ends. Between the ends, a cross-connected structure is placed. To extend the output levels of this inverter, we simply connect more cells in the space highlighted with dashed lines. Noticing that the input voltages of the capacitors are not equal, the topology is considered asymmetrical. The main benefit of this topology is the ability to boost the input voltage using charging capacitors and accumulating their voltages to produce higher levels. This boosting feature allows for the removal of transformers and presents a solution for bulky, heavy magnet cores. In the studied example in the article, the authors simulated and validated a topology of 7 levels. The circuit is composed of 6 capacitors which charge and discharge in different patterns which require balancing. The circuit is also composed of 22 switches. Meanwhile, to produce the same levels using the classical T-type inverter, we need the same number of capacitors but only 14 controllable switches.



2014

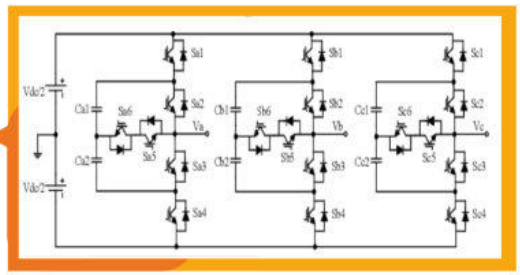
Novel efficient T-type 3L-NPC

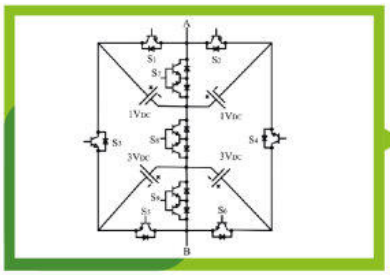
In [8] reserchers proposed a renewable energy friendly circuit. for renewable energy system is proposed to achieve both low conduction losses and switching losses with at switching frequency.

2016

Nested T-Type

[9] Presents a novel Nested T-Type (NT-Type) four-level inverter for high power and medium voltage applications. Its main advantages is operating over a wide range of voltage.





2017

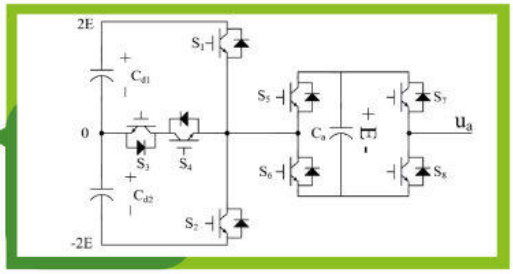
ST-Type

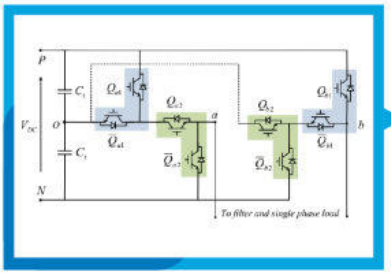
In [10] paper introduces Square T-Type (ST-Type) a new module for asymmetrical multilevel inverters with the low number of components. The module is a square combination of two back-toback T-type inverters and some other switches.

2017

T²C T-type

Paper [11] presents a hybrid seven-level converter based on T-type converter called (T²C) and H-bridge (HB) cascaded suitable for low-voltage and high power density applications.





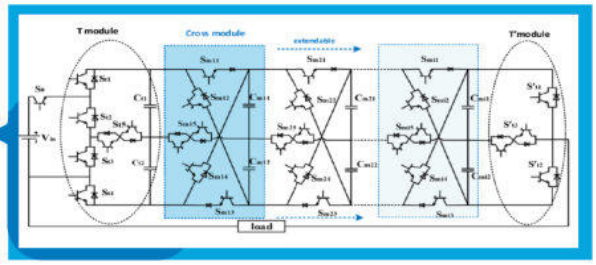
2018

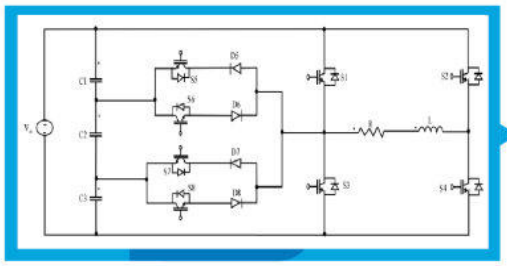
Modified T-type

In paper [12], two new three level inverter legs are derived by modifying the conventional three level T-type topology with common emitter and common collector configurations respectively

2018
Cross-connected T-type

This study [13] presents a new topology of switched-capacitor (SC) multilevel inverter, which is designed based on series connection of the capacitors that charged by input DC sources through a SC network.



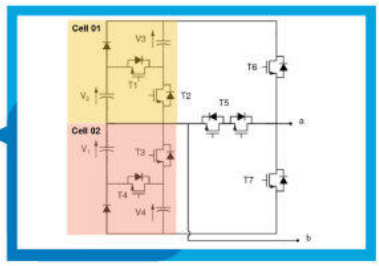


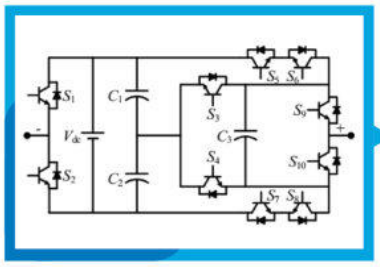
2018
New 7-level MLI

In the topology of [14], the proposed inverter contains a full H bridge connected to an auxiliary circuit of switches. The contribution of this topology compared to the classical T-type is in the auxiliary switches circuit.

2018
Novel T-type

[15] Presents and validates a novel transformerless single-phase 5-level inverter with a complete DC bus utilization for PV applications.



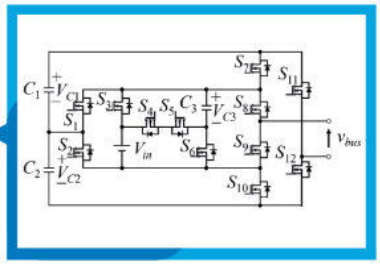


2018
7-level MLI

In [16], Based on the switched-capacitor (SC) principle, a seven-level inverter is proposed, which can synthesize seven levels containing a single dc source

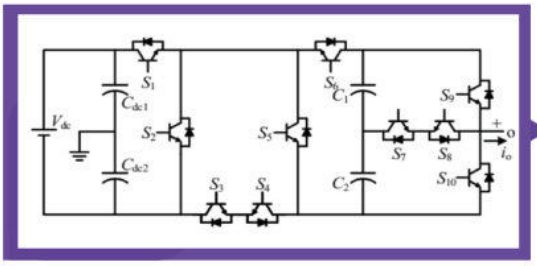
2018
Boost-Type SC MLI

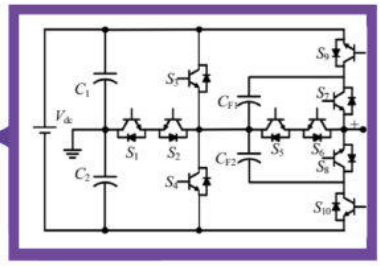
In [17], A new boost type multilevel inverter using switched capacitor structure is proposed. The main feature of the proposed inverter is boosting and multilevel output with small number of components



2019
DTT-7L MLI

In [18], an alternative ANPC topology is established called dual-T-type seven-level boost MLI. with its self-voltage balancing capability it can achieve a voltage-boosting gain of 1.5.



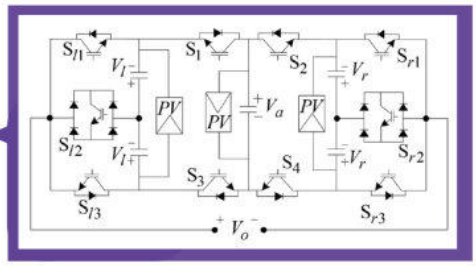


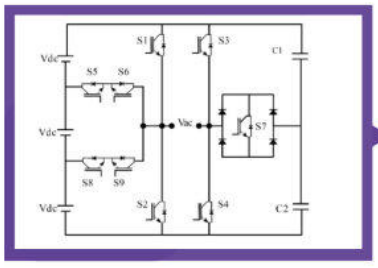
2019
Boost MLI

The prominent feature of the presented topology in [19] is boosting the input voltage vdc to an output level of 1.5 vdc.

2019
Modified T-type

In [20], authors propose a modular multilevel inverter. The circuit is well suited for photovoltaic applications. in the example circuit treated, the circuit module can include 3 PV panels.



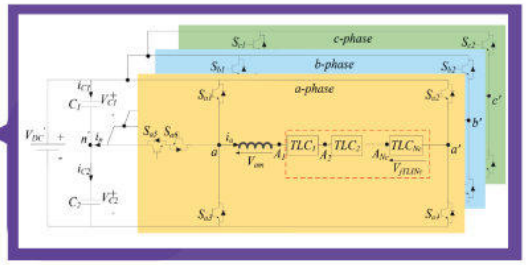


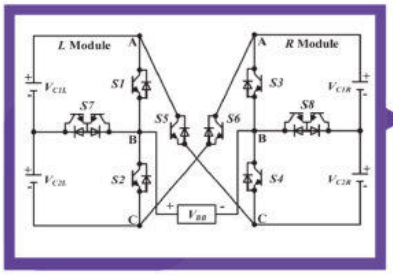
2019
Hybrid T-type

Paper [21], proposes a hybrid multilevel inverter topology suitable for isolated supply electric systems. The proposed system is a congregation of T-type and Active Neutral Point Clamped (ANPC) converter modules.

2019
Hybrid N-Level T-Type

In [22], A Hybrid N-Level T-Type Inverter topology is presented. It is composed of a multilevel T-type converter and a set of two-level converters, connected according to an open-end winding configuration to the supplied AC load (machine).





2019

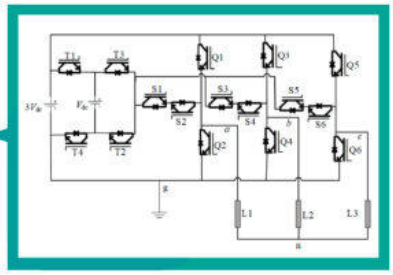
CT-Type

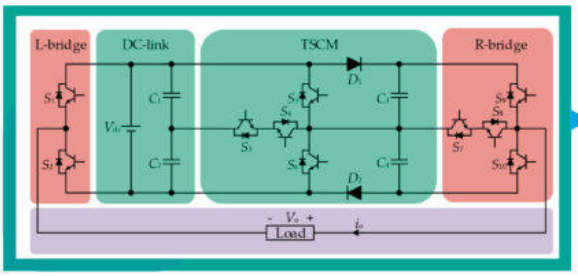
The article [23] introduces a novel configuration of multilevel inverter with low number of power electric components. The inverter is a combination of two back to back T-type modules using two cross-connected switches.

2020

Novel T-Type

This research [24] proposes a four-level T-type inverter that is suitable for low-power applications. The presented topology outranks other types of inverters in terms of the number of switches,





2020

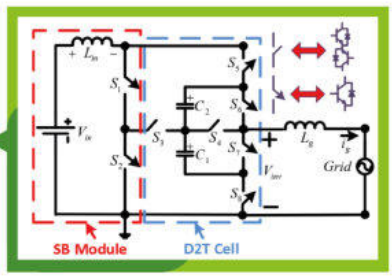
T-Type SC

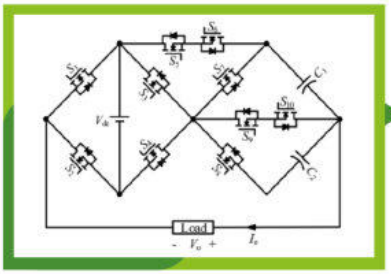
In [25], A Generalized Multilevel Inverter Based on T-Type Switched Capacitor Module with Reduced Devices is presented

2021

SBD2T

In [26], researchers present design, control, of a Novel Grid Interfaced Switched-Boost Dual T-Type Five-Level Inverter With Common-Ground Concept. the example studied is five-level output voltage generation.

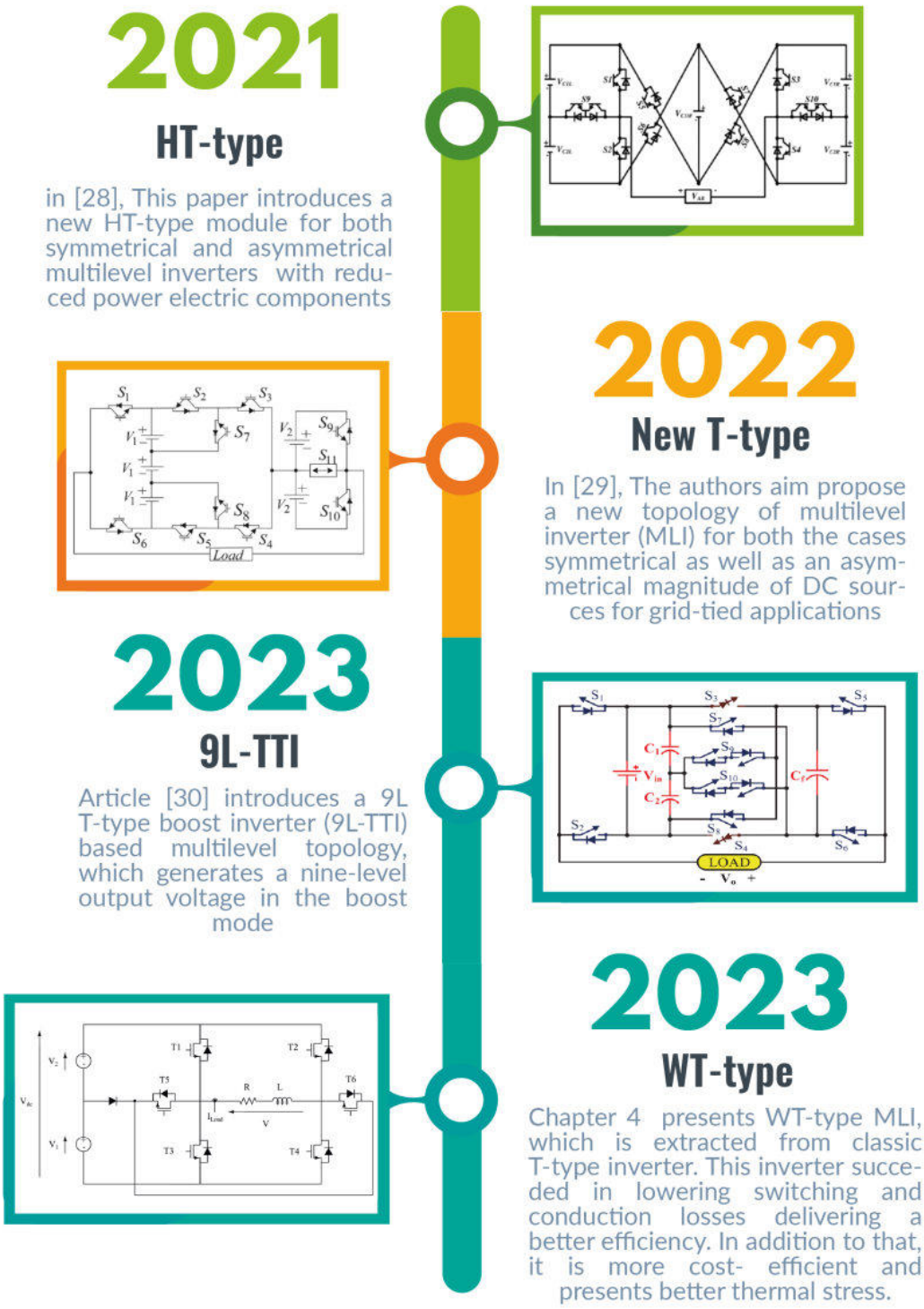




2021

Novel SC T-type

In [27], authors propose novel T-type multilevel inverter (MLI) based on the switched-capacitor technique. The proposed achieves lower switches voltage stress also has a voltage boost capability



In the topology of [14] (2018-3) Figure, the inverter is designed of two parts: a full H-bridge and an auxiliary circuit of switches. The contribution of this topology compared to the classical T-type is in the auxiliary curcuit. In this later switches are replaced with

two parallel connected branches of a switch (IGBT, for example) connected in series to a diode. The source of IGBT is connected to the diode anode in the first branch. Contrary to the second branch, where the drain is connected to the diode cathode as shown in the timescale. This article studied a 4-level topology of the proposed inverter, it consists of 8 IGBTs in addition to 4 diodes. For the same level, classical T-type inverters contain 8 IGBTs. additional diodes may reduce the cost efficiency of the proposed inverter. The DC-link input voltage is shared among the capacitors, which means they require balancing.

In [15] (2018-4), the authors propose a topology consisting of a half-bridge-based T-type inverter connected to 2 cells highlighted in red and yellow as depicted in the Figure. Each cell is composed of 2 capacitors, 2 switches (IGBTs), and a single diode. With the help of the control technique, this topology uses the switched-capacitor principle. In this mode of operation, the capacitor is connected to switches, which turn on and off in different patterns, resulting in a symmetrical charging and discharging of the capacitor, hence, self-balanced capacitors. In the 3-level topology of the classical T-type, we need 6 switches and 2 capacitors. Meanwhile, in the example studied in this article, for the same number of levels, we need 8 switches, 4 capacitors, and 2 diodes. The overall component count of the proposed inverter makes it less cost-efficient.

In the article [16] (2018-5), the authors propose an inverter based on switched-capacitor mode as we can see on the timescale. We notice that this topology doesn't include an H-bridge. The studied example of the inverter is a 4-level topology. It includes a single DC source, whose voltage is shared between 2 capacitors (C_1, C_2). Furthermore, we have a third floating capacitor C_3 that offers the feature of boosting the input voltage with a ratio of 1.5 Vdc. The classical 4-level T-type inverter is composed of 8 switches. Meanwhile, the studied inverter contains 10 switches.

In the article [17] (2018-6), researchers present a boost multilevel inverter as presented on the timescale. The research treats an example of a 5-level inverter. This later consists mainly of three parts, the input 2 capacitors on the left-hand side, 2 switches on the right-hand side, and The auxiliary circuit that connects the 2 previous parts and represents the boosting body. At each sequence, capacitors c_1, c_2, and c_3 are charged and discharged and arranged in such a way as to produce higher levels than the input. The article details the turning off and on sequences that correspond to a boosting ratio of $4v_{dc}$.

In [18] (2019-1), the inverter proposed by researchers is called dual-T-type 7-level boost ANPC. This inverter is composed of a half-bridge-based T-type converter on the left-hand side and a particular circuit shown in Figure. The inverter contains 4 capacitors two for the DC-link, and two capacitors for the second part. These two later are floating

capacitors used to boost the input DC-link with a ratio of 1.5. This can be achieved by charging the floating capacitor c_{f1} from the DC-link at a specific instant for producing levels 0.5vdc and -1.5vdc. Likewise, charging c_{f2} for generating -0.5vdc and 1.5vdc. These capacitors c_{f1} and c_{f2} operate symmetrically for each half-cycle as detailed in the cited article. which results in a self-balance of their voltages.

In [19] (2019-2), researchers propose an inverter to boost the input voltage. This inverter contains 3 main parts as shown in the circuit on the timescale. Two capacitors connected directly to the input vdc. On the right-hand side, is a half-bridge-based T-type inverter. the third part is a network of bidirectional switches linked between the 2 remaining parts. The prominent feature of the presented topology is boosting the input voltage vdc to an output of 1.5 vdc. Not only that, the maximum reverse blocking voltage on the switches is only vdc. The studied example of this inverter is a 7-level circuit. It generates the following levels: 1.5Vdc, -Vdc, -0.5Vdc, 0, 0.5Vdc, Vdc, and 1.5Vdc. For the 4 capacitors, a self-balancing strategy is applied by the control circuit such that: C_1 and C_2 are charged to half the input voltage vdc/2 and they are discharged symmetrically during the positive and negative half-cycles.

In [20] (2019-3), authors propose a modular multilevel inverter. The circuit is well-suited for PV applications. In the example studied in the article, the circuit module can be connected to 3 PV panels as we can see in this Figure. This circuit is composed of 2 half-bridge-based T-type inverters with 2 capacitors and an auxiliary circuit placed on the right-hand and left-hand sides. These parts are connected through a network of switches. With 10 switches and 8 diodes, the converter can generate 15-level voltages. The main drawback of this topology is that it needs more than one input source to charge and discharge the capacitors.

In [21] (2019-4), the authors present a hybrid topology of multilevel inverters. This configuration consists of two parts: a half-bridge-based T-type multilevel inverter with two capacitors c_1, c_2, the second part is a circuit composed of 3 dc inputs as presented in this Figure. The case studied in this publication is a 6-level example that generates: $\pm V/6$, $\pm V/3$, $\pm V/2$, $\pm 2V/3$, $\pm V$, and 0. It is composed of 9 switches, 4 diodes, 2 capacitors, and 3 voltage sources. The two capacitors of the T-type part require balancing, which is achieved by a proper charge and discharge of the capacitors through the control technique.

In [22] (2019-5), researchers propose a configuration called a hybrid N-level T-type inverter. The overall circuit is composed of a full-bridge-based T-type multilevel inverter. The prominent idea about this inverter is connecting a series of modules to the load side. These modules are composed of H-bridges connected in series depending on the desired

number of levels. The circuit of this inverter is shown in this Figure. In this research, a 5-level circuit was studied and generates Vdc, Vdc/2, 0, -Vdc/2, and -Vdc.

In [23] (2019-6), researchers introduced a hybrid circuit of multilevel inverters named Cross-Switched Multilevel Inverter (CT-MLI) as shown in the timescale. The circuit consists of 3 parts, two half-bridge-based T-type modules on the left-hand (L module) and right-hand sides (R module). The third part is connected between the two, which is a cross-switched circuit. For a higher level of this inverter, more modules are connected in series. In the studied example, the circuit consisting of 10 controllable switches, 4 capacitors, and 2 voltage sources operates in asymmetrical mode and can produce 9-levels. The same previous components count produces 5 levels in symmetrical mode. For a 5-level output of the classical symmetrical T-type multilevel inverter, we need only 10 switches.

In [24] (2020-1), researchers propose a circuit for low-power applications multilevel T-type inverter named LT^{2}C as shown on the timescale. The topology of this inverter is similar to classical T-type multilevel inverters but differs in the auxiliary circuit. This later is a circuit containing unequal DC voltage sources. The presented example is a 3 phase circuit based on a bridge. The three upper and 3 lower switches operate in a complimentary manner. The topology explained in the paper is of a 4-level asymmetrical topology. The single-phase topology of the presented inverter consists of 10 switches and 2 voltage sources with different voltage values.

In [25] (2020-2), the paper proposes a modular topology of multilevel inverters with lower component numbers. The studied circuit is a 5-level inverter with 10 switches, 2 diodes, 4 capacitors, and a single DC voltage source as depicted in the Figure. It can boost the input source voltage with a ratio of 2 as follows: $\pm 2Vdc$, $\pm 1.5Vdc$, $\pm Vdc$, $\pm 0.5Vdc$ and 0. Regarding the circuit structure, the topology is composed of 2 half-bridge-based T-type inverters as highlighted in red, linked through 2 diodes to the part highlighted in green which is a circuit with 4 capacitors. These later capacitors require balancing for correct operation, which is achieved by a self-balancing technique that guarantees proper charging and discharging of capacitors.

In [26] (2021-1), researchers present a hybrid T-type multilevel inverter to reduce the component count as shown in this Figure. This multilevel inverter is an improvement of the converter presented in [23] (2019-6). The circuit of the proposed inverter is composed of 2 main parts: an SB module (switched-boost) highlighted in red, and Dual T-type modules (D2T) highlighted in blue and a load. With a component count of 12 switches and 5 voltage sources, the studied topology is capable of producing 6 levels in a symmetrical

mode of operation. The topology can also operate in asymmetrical mode where it can give 21 levels. The control technique employed in the presented article is Selective Harmonic Elimination PWM (SHE-PWM), which is a voltage control-oriented technique that takes into account the optimization of voltage qualities over the current.

In [27] (2021-2), the authors present a novel T-type multilevel inverter based on the switched-capacitor technique that can boost the input dc voltage with a ratio of 3vdc/2. This inverter contains a half-bridge-based T-type inverter on the right-hand side, linked to a network of switches, making the total count 10 switches, a single DC voltage source, and 2 capacitors. The example studied in this paper is a 4-level inverter. As the 2 capacitors require balancing The authors used the control technique PD-PWM to do so. As shown in the timescale, because C_1 and C_2 are connected in series, C_1 is charged when the output level is Vdc/2 and discharged during the levels -Vdc/2 and - 3Vdc/2. Whereas C_2 is charged when the level is -Vdc/2 and discharged at Vdc/2 and 3Vdc/2. As can be seen, the charging and discharging states of the two capacitors are symmetrical within one cycle. That is to say, C_1 operates at the negative half cycle; after that, its voltage will drop and the voltage of C_2 will rise then they switch roles as shown in Figure 4.2. The voltages of c_1 and c_2 return to their initial states after a cycle. As a result, the voltages of the two capacitors are balanced, thus, they are in a "self-balanced" state.

In [28] (2021-3), authors propose a novel A hybrid T-type multilevel inverter called HT-type. The presented topology can operate in symmetrical and asymmetrical modes. It contains 12 switches and 5 voltage sources as shown in this Figure. In the example treated in this paper, the inverter operated in symmetrical mode to generate 6 levels, and in asymmetrical mode to produce 12 levels. In symmetrical mode, this inverter needs 12 switches to generate 6 levels. For the same levels, classical T-type inverters need the same switch count.

In [29] (2022), researchers propose a novel symmetrical and asymmetrical multilevel inverter to reduce the number of switches. The presented topology is composed of a half-bridge-based T-type inverter on the right-hand side connected to a proposed circuit. It consists of 12 switches and 5 voltage sources as depicted on the timescale. The structure of the multilevel inverter is well-suited for PV sources. According to the research results, the inverter showed good THD values of output voltages at different levels: 9-level, 15-level, and 21-level,where it had a THD of 9.11%, 5.28%, and 3.67% respectively. By comparing the symmetrical operation of this inverter with the classical T-type multilevel inverters for a 21-level output, we need the same switch count.

In [30] (2023-1), a new multilevel inverter is proposed with the ability to boost the input voltage. This multilevel inverter aims to reduce the number of devices and reverse

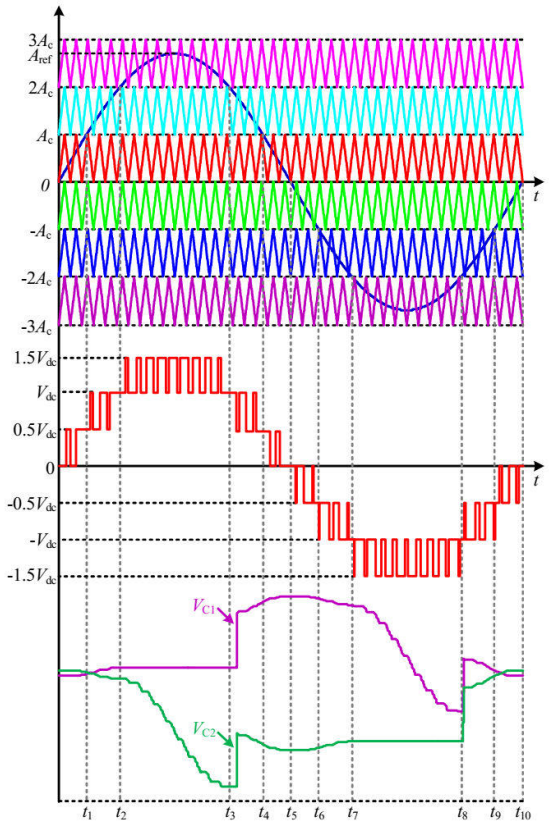


Figure 4.2 – Symmetry of charge and discharge of capacitors C_1 and C_2 for a self-balanced operation, Figure source [27].

blocking voltages. The structure of this inverter is composed of 8 unidirectional switches and 2 bidirectional switches, for a total of 12 switches as shown on the timescale. It contains 2 capacitors C_1 and C_2 at the DC-link, and the floating capacitor C_f which is considered as a switched-capacitor unit. This multilevel inverter can boost the input DC-link with a ratio of 2 vdc. By comparing the studied example that contains 12 switches, classical T-type multilevel inverters need only 10 switches to produce the same voltage levels.

4.3 Proposed multilevel inverter

4.3.1 Optimisation steps

The proposed topology is derived from the classical T-type converter [8]. They both share a full H-bridge but differ in the auxiliary circuit that generates sub-levels. Because of the shape of the auxiliary circuit, the proposed inverter is named Wings T-type multilevel inverter (WT-type) and shown on the timescale. The goal of the WT-type is to reduce

the number of switches of the classical T-type. As a result, reducing the cost and creating the potential to improve its efficiency. In the classical T-type multilevel inverters, The auxiliary circuit contains bidirectional switches usually connected source-to-source. This part contains a large number of IGBTs. Therefore, the number of IGBTs in this circuit is cut to half in the proposed topology with the introduction of ultrafast diodes. the construction steps of this circuit are explained in the next paragraphs.

Figure 4.3, shows a nine-level T-type multilevel inverter. The auxiliary circuit noted with (1), connects 4 dc voltage sources to the H-bridge. This later circuit is composed of bidirectional switches that control the flow of current in both directions and hence, produce the negative and positive sublevel voltages.

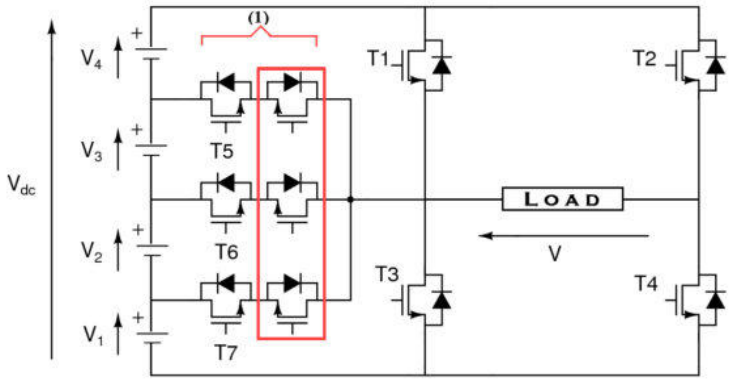
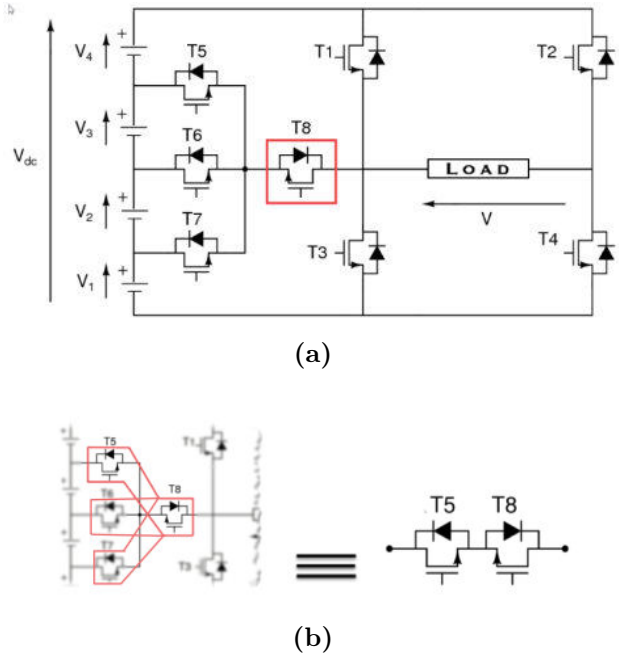


Figure 4.3 – Cumbersome switches in the auxiliary circuit of the classical T-type inverter.

To reduce the number of switches in area (1),The idea is to substitute IGBTs within the red frame in Figure 4.3 with a single common IGBT as shown in Figure 4.4a. This IGBT is meant to play a source-to-source connection and form a bidirectionality with each switch T_5, T_6, and T_7 as shown in Figure 4.4b. The new obtained form must preserve a controllable current flow in both directions.



(a)

(b)

Figure 4.4 – Bidirectionality creation of the switches (a), substitution of 3 switches with 1 switch(b).

At this stage, the resultant circuit must comply to the laws of the interconnection of sources: a voltage source should not be short-circuited and can be open-circuited, whereas current sources should not be open-circuited and can be short-circuited as shown in Figure 4.5a, 4.5b.

(a) (b)

Figure 4.5 – The forbidden states of connections in power electronics (a), (b).

By analysing the operation of the resultant circuit as depicted in Figure 4.6, when one of the IGBTs T_5 or T_6 is activated, a short-circuit of voltage sources V_2 and V_3 occurs due to the circulation of current through body diodes of T_7 and T_6 respectively as shown in Figure4.6.

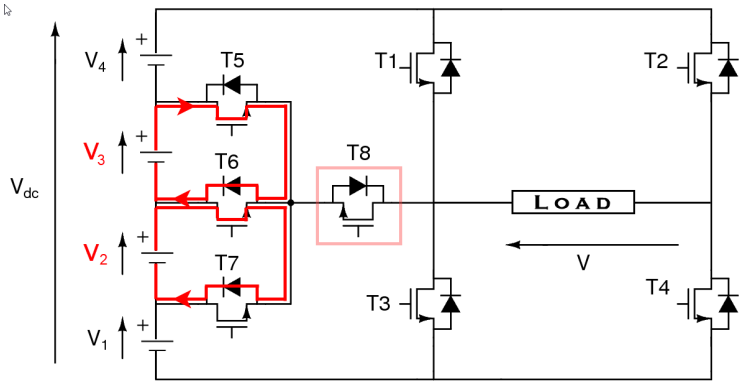


Figure 4.6 – Short-circuit challenge in the first optimization step.

To control the circulation of current in the reverse direction to sources V_2 and V_3, we introduce diodes to each switch T_5, T_6 and T_7 as shown in Figure 4.7. hence, all voltage sources are protected.

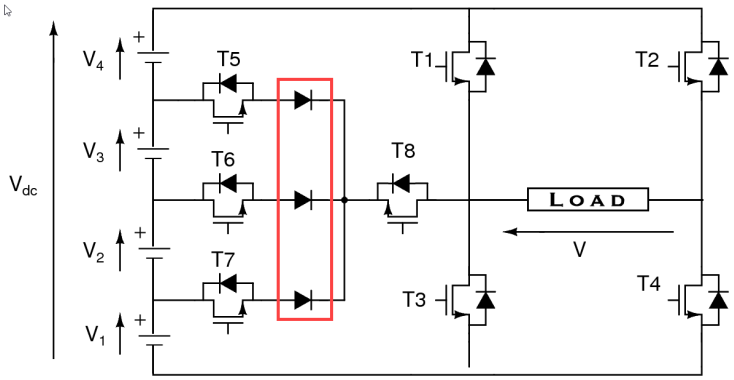


Figure 4.7 – Proposed solution to surpass the short-circuit.

Yet, the present form of the inverter's circuit allows the current to only circulate in a direction and not in the reverse one. This means that it can only generate the positive waveform and block the negative one. To guarantee a circulation of current in both directions we introduce a controllable switch T_9 connected as shown in Figure 4.8.

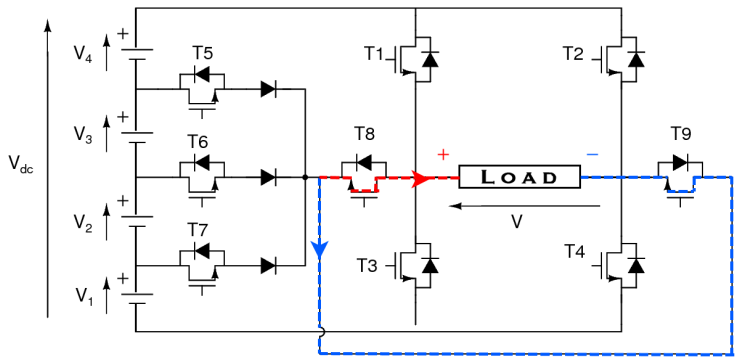


Figure 4.8 – Resolving the negative sublevel current blocking.

4.3.2 Switching states

The circuit of WT-type multilevel inverter is presented in Figure 4.9. The 3-level topology is presented in Figure 4.9a. For output levels greater than 3, Figure 4.9b illustrates the general structure for n-levels, where n $>$ 3.

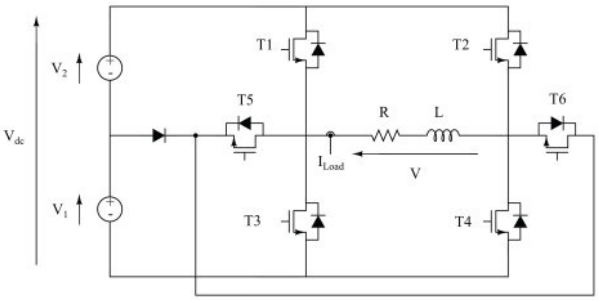


Figure 4.9 – Proposed Three-level T-type topology (a), the circuit of n-level proposed T-type topology(b)

We study the voltages generation of a 3-level single-phase topology of WT-type multilevel inverter. The following switch combinations synthesize the output levels as follows:

(1) For the level +Vdc , T_1 and T_4 are **on**.

(2) For the level +Vdc/2 , T_4 and T_5 are **on**.

(3) For the level 0, there are two combinations:

- The upper switches of the H-bridge T_1 and T_2 are **on** .
- The lower switches of the H-bridge T_3 and T_4 are **on**.

(4) For the level -Vdc/2, T_3 and T_6 are **on**.

(5) For the level -Vdc, T_2 and T_3 are **on**.

Figure 4.10 depicts the 6 possible switching sequences that correspond to the output levels. It can be observed that the H-bridge part generates the upper levels ±Vdc, while the auxiliary circuit generates the sublevels ±Vdc/2. Table 4.4 details the on and off state of each switch for each level. For the level 0, we have two combinations as shown in cases (3) and (4) in Figure 4.10.

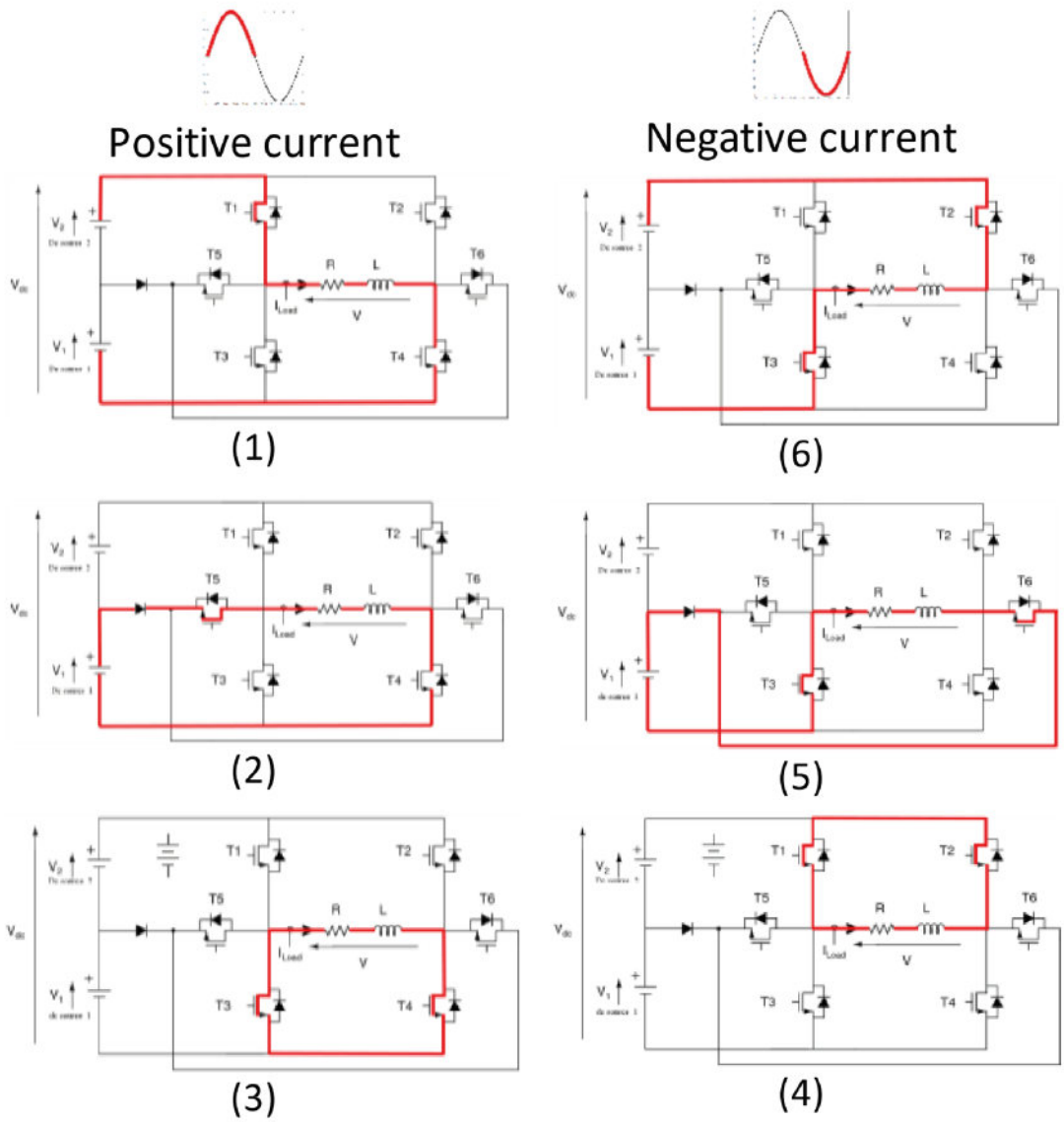


Figure 4.10 – The states of each level of the 3-level proposed inverter

In table 4.3, we introduce a comparison of WT-type multilevel inverter among various types of multilevel inverters. it introduces mathematical expressions of multiple quantities like the number of capacitors, diodes, IGBTs, and drivers. These expressions are as function of n which refers to the number of levels. The expressions in last line refer to

Table 4.3 – Number of various components of the converter as a function of the number of levels n.

Topology	NPC [31]	FC [32]	Ttype [33]	K-type [34]	WT-type
Topology name	Neutral Point Clamped	Flying Capacitor	T-type	k-type	Wings T-type
DC-link capacitors	$\frac{n}{2}-1$	$\frac{n}{2}-1$	$\frac{n}{2}-1$	$2[\frac{n-2}{12}+1]$	$\frac{n}{2}-1$
Diode	n -1	0	0	0	n-4 if $n \leq 5$ $\frac{n}{2}-1$ if $n \geq 5$
Switches Ns	2(n-1)	2(n-1)	n-1	14 $[\frac{n-2}{12}+1]$	n+1 if $n \leq 7$ n-p, p $\in$ N if $n \geq 7$
Drivers	n- 1	2(n-1)	n+1	11 $[\frac{n-2}{12}+1]$	n-4 if $n \leq 5$ $\frac{n}{2}-1$ if $n \geq 5$
total	4(n-1)+$\frac{n}{2}-1$	4(n-1)+$\frac{n}{2}-1$	2(n-1)+ $\frac{n}{2}-1$	32 $[\frac{n-2}{12}+1]$	n-2+n-p p $\in$ N if $n \geq 7$

Table 4.4 – The ON and OFF states of each switch of the 3-level WT-type multilevel inverter.

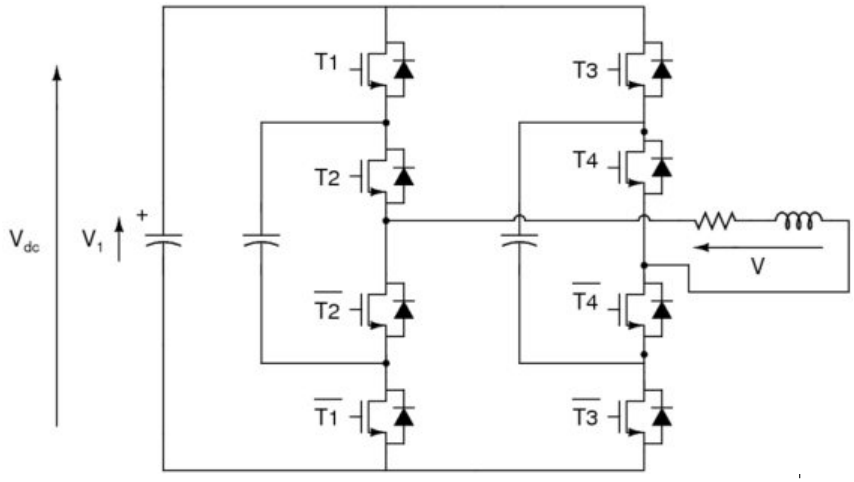
T1	T2	T3	T4	T5	T6	Vl
1	0	0	1	0	0	V1+V2
0	0	0	1	1	0	V1
0	0	1	1	0	0	0
1	1	0	0	0	0	0
0	0	1	0	0	1	-V1
0	1	1	0	0	0	-V1-V2

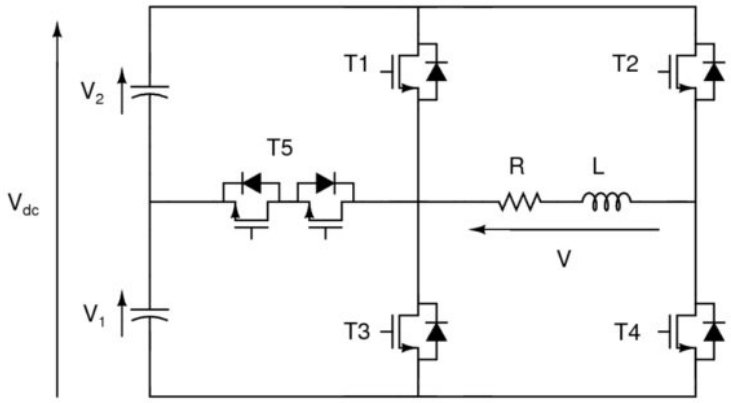
the total component count. Figure 4.12 illustrates curves of the total components count for each multilevel inverter types.

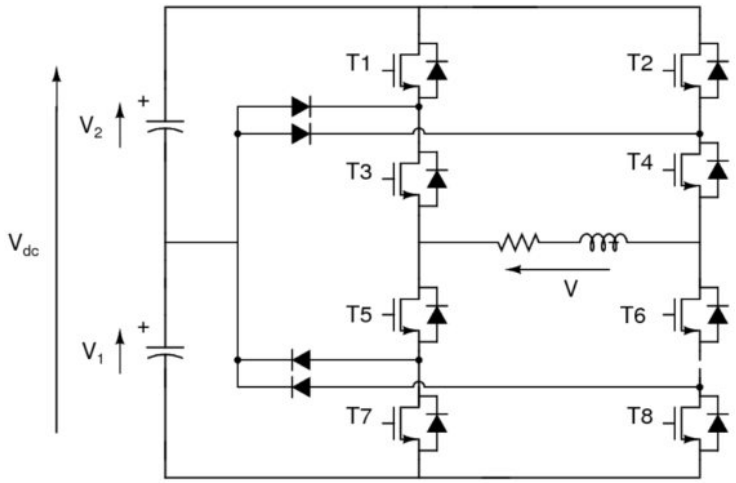
4.3.3 Intrinsec features

4.3.3.1 Number of components

Figure 4.12 presents the components number of various multilevel inverters circuits namely: NPC, FC, Ttype, and WT-type. These configurations are compared in terms of the total number of components which include capacitors, diodes, and IGBTs. As we observe, the NPC structure has the highest number of components. The second highest number of components is of the FC-MLI. The lowest component count is related to the classical T-type with the proposed WT-type multilevel inverter.


T1
T3
T2
T4
V_dc
V_1
+
V
T2
T4
T1
T3


T1
T2
V_2
T5
R
L
V_dc
V
V_1
T3
T4


T1
T2
V_2
+
T3
T4
V_dc
V
T5
T6
V_1
+
T7
T8

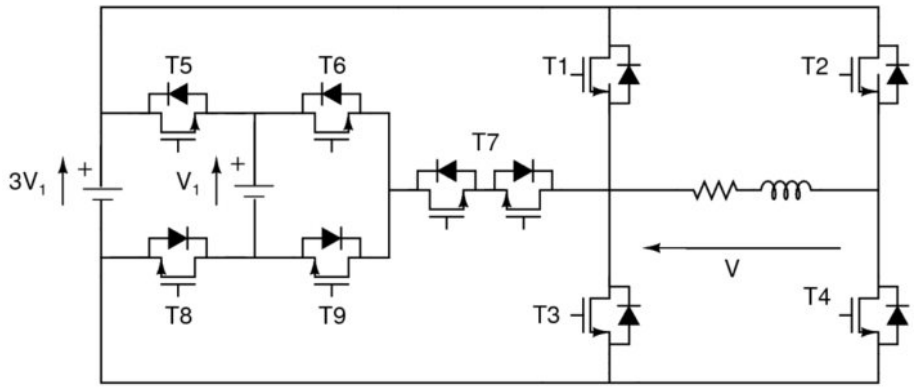


Figure 4.11 – single phase converters in compared to the studied multilevel inverter

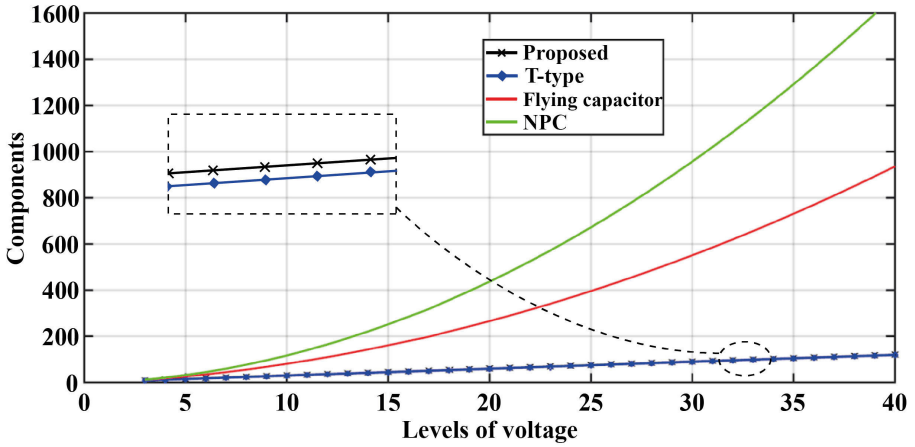


Figure 4.12 – Number of components in other multilevel topologies (NPC[3], FCC[3],T-type[8] and proposed converter).

4.3.3.2 Cost

The previous components give an idea about the cost of the inverter. To evaluate the cost-efficiency of the WT-type multilevel inverter we compare its cost with the cost of the classic T-type multilevel inverter. We list the components of the two inverters for various levels namely: switches (IGBTs, MOSFETs,...), diodes, and capacitors.

The two multilevel inverters share the same number of capacitors, therefore, capacitors are not included in the comparison. Table 4.5 shows the details of this comparison. We consider the same price of components such that, the power switch is a MOSFET (20N60) with a unit price of 1.05 US $, whilst, the ultrafast diode (MUR860) costs 0.135 US $ per unit. These prices can be found on any shopping website.

From the table, we notice that the proposed converter has a cost close to the classical converter in the 3-level topology. The cost however becomes remarkably lower than the

Table 4.5 – Overall cost of components between the classical and its derived converter

Levels	3		5		41	
	Mosfet	Diode	Mosfet	Diode	Mosfet	Diode
Proposed topology	6	1	9	3	25	19
	6.30 $	0.13$	9.45$	0.4$	26.25$	2.5$
	6.43$		**9.85$**		**28.75$**	
Classical T-type [8]	6	0	10	0	42	0
	6.30	0	10.5	0	44.1	0
	6.3 $		**10.5 $**		**44.1$**	

classical T-type as we increase levels, where at 41-level, WT-type becomes 35% more cost-efficient than T-type multilevel inverter.

4.3.3.3 Thermal stress (switching losses)

The temperature has a significant impact on the reliability of power components. it can increase due to various factors like switching, conduction losses, operation frequency, and even the intrinsic form of the topology.

High temperatures are undesirable, particularly in commercial devices where it increases the volume of the cooling system and thus the volume and the price of the device. Therefore, industrial manufacturers endeavour to reduce temperature, one classical solution is to connect a second switch in parallel so that the burden is divided and temperature rests at low rates.

To evaluate the heat stress of WT-type multilevel inverter, we operate the WT-type and classical inverters under the same operation conditions: sampling time, input voltage, load values, references, and control algorithm. After that, we count the sum of switching events that occur in each inverter (diode and IGBTs) which indicates the amount of heat dissipated. The experimental results are illustrated with a colour Figure as depicted in Figure 4.24 and interpreted in the results section.

4.3.3.4 Losses

Conduction losses make up the higher share of the losses in power converters. Therefore, it gains special attention in the evaluation of inverters.

Commonly, the presence of diodes in a circuit relates to higher conduction losses, therefore the presence of MOSFETs or IGBTs is rather preferable. If we project this view on the studied topology, we see that the WT-type topology contains more diodes than the classical one, which gives the impression that it has higher conduction losses.

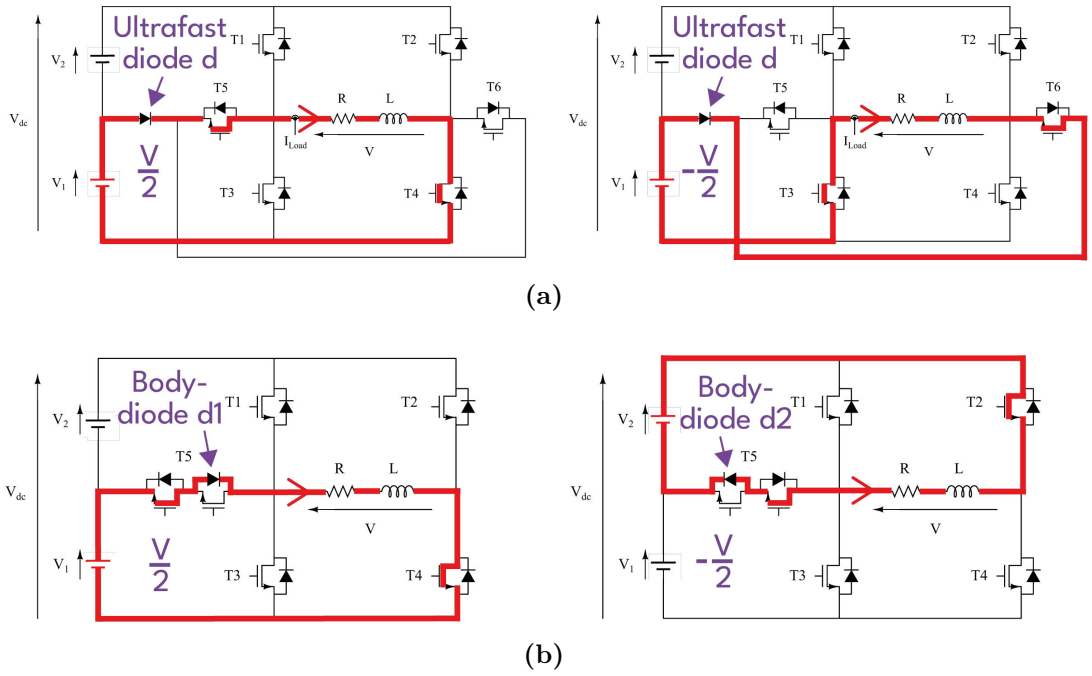


Figure 4.13 – Current trajectory at the generation of the level of voltage Vdc/2 of the studied multilevel inverter (a), classic T-type (b).

This however is incorrect. The WT-type and T-type generate the upper levels ±vdc similarly, but they differ in sub-levels $\pm\frac{Vdc}{2}$. Figure 4.13a shows the trajectory of current at the generation of levels $\pm\frac{Vdc}{2}$ in the proposed inverter while Figure 4.13b shows the trajectory of current at the generation of the same levels in the T-type inverter.

In Figure 4.13a, when the WT-type generates $\frac{Vdc}{2}$ the current passes through the ultrafast diode and MOSFETs T_5 and T_4. While to generate -$\frac{Vdc}{2}$, the current passes through the ultrafast diode and MOSFETs T_6 and T_3. For the classical T-type, Figure 4.13b indicates that to produce $\frac{Vdc}{2}$ the current flows through T_5 (body-diode d1 with MOSFET T_5) and T_4 and to produce -$\frac{Vdc}{2}$ through T_5 (body-diode d2 with MOSFET T_5) and T_2 . The number of these components is organized in table 4.9.

From table 4.9, we notice that current flows through some number of diodes that are similar in both multilevel inverters. Furthermore, thanks to the fact that the characteristics of ultrafast diodes (WT-type) are much better than body diodes (T-type), we deduce that the proposed multilevel inverter improves the conduction losses of the classic one as explained in the next section.

To evaluate the performance of the two types of diodes (ultrafast and body-diodes) within the inverter, we quantify their conduction losses and switching losses.

The average conduction losses formula is given by the relation [35]:

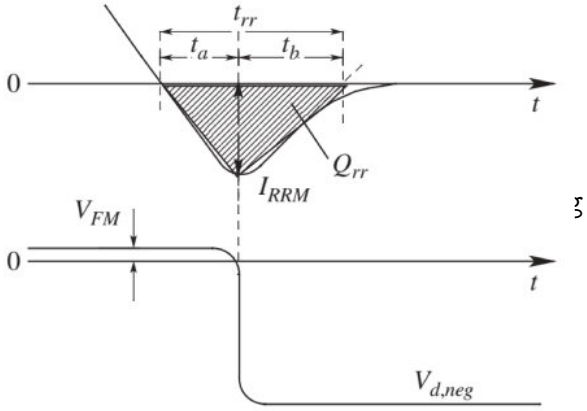


Figure 4.14 – Reverse recovery characteristic of a diode, source [35].

Table 4.6 – Number of components through which the current passes while generating each level

Levels	Proposed MOSFETs	T-type MOSFETs	Proposed Diodes	T-type Diodes
V	2	2	0	0
V/2	2	2	1	1
0	2	2	0	0
-V/2	2	2	1	1
-V	2	2	0	0

$$P_{d,forward} = V_{FM} \times I_{avg} \times (1 - d) \tag{4.1}$$

V_{FM} is the forward voltage drop, I_{avg} is the average current and d is the duty cycle. From equations 4.1 the characteristics of forward voltage V_{FM} differ from one diode to another. By looking at datasheets of multiple ultrafast diodes and body-diodes, we notice that the forward voltage V_{FM} of the ultrafast diodes is remarkably lower than that of the body diodes. Figure 4.15, presents multiple pieces of information extracted from datasheets of various ultrafast diodes and body-diodes (MOSFETs and IGBTs) available in the market. This Figure shows that ultrafast diodes present better technical characteristics, where the best V_{FM} value among various ultrafast diodes is O.95V, on the other hand, the best V_{FM} value for body-diodes was no less than 1.4V. Therefore, according to 4.1, for a diode operating under the same duty cycle, passing the same current, the lower forward voltage V_{FM} the lower forward losses the diode dissipates.

For switching losses, the reverse recovery time t_{rr} of a diode plays a key role in the amount of switching losses dissipated. Therefore, from Figure 4.15 ultrafast diodes present better values of reverse recovery time as shown in the blue squares. As we notice, the

Table 4.7 – Reverse voltage value applied to each component of the proposed inverter

State	Level	T_1	T_2	T_3	T_4	T_5	T_6	d
1	+Vdc	0	Vdc	Vdc	0	0	Vdc	Vdc/2
2	+Vdc/2	Vdc/2	Vdc	Vdc/2	0	0	Vdc/2	0
3	0	Vdc	Vdc	0	0	Vdc/2	Vdc/2	0
4	0	0	0	Vdc	Vdc	0	0	Vdc/2
5	-Vdc/2	Vdc	Vdc/2	0	Vdc/2	Vdc/2	0	0
6	- Vdc	Vdc	0	0	Vdc/2	Vdc/2	0	0

worst and best reverse recovery time value t_{rr} of body diodes is 600ns – 370ns and for ultrafast diode is 75ns - 15ns. The equation of the switching losses can be expressed as follows [35]:

$$P_{d,sw} = (\frac{1}{2} I_{RRM} \times t_b) \times V_{d,neg} \times f \tag{4.2}$$

I_{RRM} is the peak current of the overshoot as shown in Figure 4.14, t_b is the interval shown in Figure 4.14 and $V_{d,neg}$ is the reverse blocking voltage as shown in table 4.7. In the light of equation 4.2, under the same operation condition of frequency, reverse voltage: a longer t_{rr} means a longer t_b and thus larger $P_{d,sw}$ switching losses.

From this section, we notice a remarkable advantage of ultrafast diodes over body-diodes, that is to say, an advantage of WT-type that uses ultrafast diodes over the classic T-type multilevel inverter that relies on body-diodes.

4.3.3.5 Additional degree of freedom

The design of inverters is realized based on specifications set in advance, such as the reverse voltage of a switch, maximum current, and losses. In some cases, many characteristics are imposed and cannot be avoided due to manufacturing obligations for instance: the characteristics of switches' body-diode (IGBT, MOSFET, ..).

One advantage of the WT-type is that it does not use a body-diode to generate levels except for level 0, it uses instead body diodes. This creates a decoupling between the characteristics of the components of this inverter. As a result, this gives the possibility to freely choose the characteristics of diodes regardless of the IGBT, particularly since ultrafast diodes present better specifications notably reverse recovery time t_{rr} and forward voltage V_{FM}.

Figure 4.15 shows values of V_{FM} and t_{rr} of body diodes (IGBTs) and ultrafast diodes covering various references as provided in the datasheets.

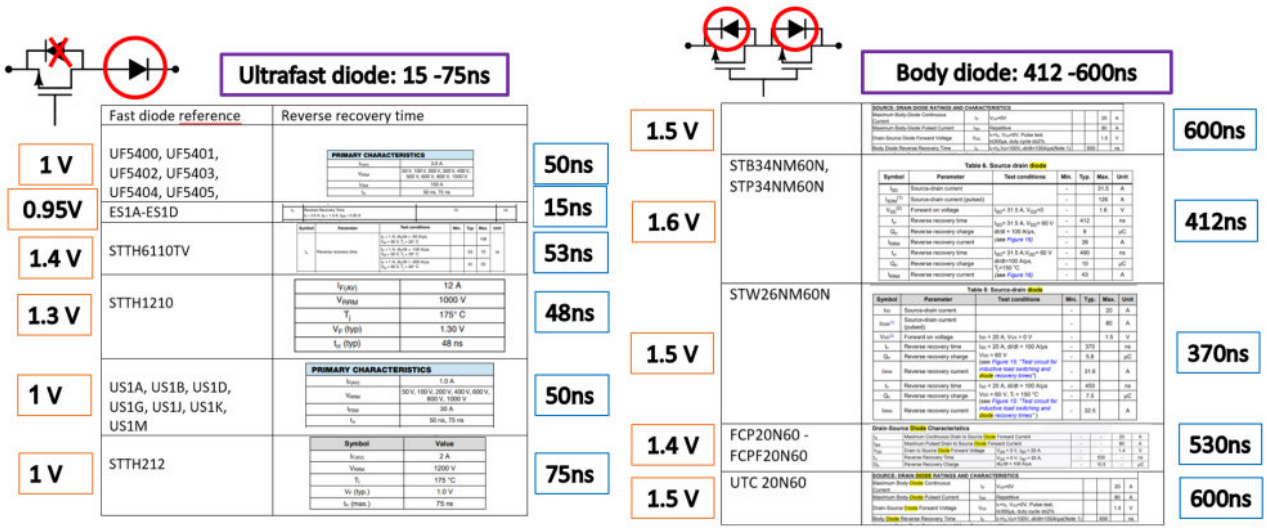


Figure 4.15 – V_{FM} and t_{rr} datasheet values of body-diodes vs ultrafast diodes according to multiple references.

4.3.4 Control of the proposed inverter

4.3.5 Mathematical model

FS-MPC technique is applied to the studied inverter. As shown in the scheme in Figure 4.16. The algorithm reads the present load voltage and current values to use them to generate possible $i_p(k+1)$ values using equation 4.4. These future values are evaluated using a cost function g as expressed in equation 4.9, to determine the optimal vector to apply in the next sampling time T_s. In our case, the DC-link voltage levels are generated using capacitors which require balancing. The mathematical model of the inverter connected to an rL load is expressed as:

$$v(t) = ri + L\frac{di(t)}{dt} + e(t) \tag{4.3}$$

After using Euler discretization, we get the equation:

$$i_p(k+1) = \frac{T_s}{rT_s + L}\left(\frac{L}{T_s}\, i(k) + v(k)\right) - e(t) \tag{4.4}$$

Where the relations between variables S_a, S_b and the switching states are expressed as follow:

$$S_a = \begin{cases} 1 & \text{if } T_1{=}1 \text{ and } T_5{=}T_3{=}0 \\ 0 & \text{if } T_5{=}1 \text{ and } T_1{=}T_3{=}0 \\ -1 & \text{if } T_3{=}1 \text{ and } T_1{=}T_5{=}0 \end{cases} \tag{4.5}$$

Table 4.8 – Output voltage vectors with their corresponding variables

Levels	Sa	Sb	Input voltage
1	1	-1	+ Vdc
2	0	-1	+Vdc/2
3	-1	-1	0
4	1	1	-Vdc/2
5	-1	0	- Vdc

$$S_b = \begin{cases} 1 & \text{if } T_2{=}1 \text{ and } T_6{=}T_4{=}0 \\ 0 & \text{if } T_6{=}1 \text{ and } T_2{=}T_4{=}0 \\ -1 & \text{if } T_4{=}1 \text{ and } T_2{=}T_6{=}0 \end{cases} \tag{4.6}$$

As a result, we can write the equation of the output voltage as:

$$v = \frac{V_{dc}}{2} + (S_a - S_b) \tag{4.7}$$

Where:

$$V_{dc} = V_1 + V_2 \tag{4.8}$$

4.3.6 FS-MPC control algorithm

The global scheme of the studied system is depicted in Figure 4.16. Through a multilevel inverter we supply an RL load. The power circuit consists of a voltage sensor and a current sensor for the load. Sensors acquire data which become inputs to the FS-MPC algorithm. As shown in the steps illustrated in the scheme of Figure 4.17 the algorithm generates the future possible 7. These later are then evaluated using a cost function g. After a minimisation process, the best state that responds to the specifications is applied in the next step T_s.

The cost function proposed in this example evaluates the errors between the predicted load currents $i(k+1)$, and the reference sinusoidal i_{ref} :

$$g = |i_{ref} - i(k+1)| \tag{4.9}$$

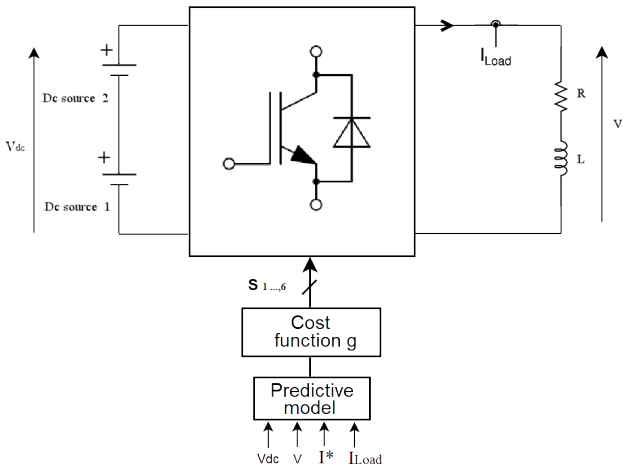


Figure 4.16 – Control strategy scheme for the proposed converter.

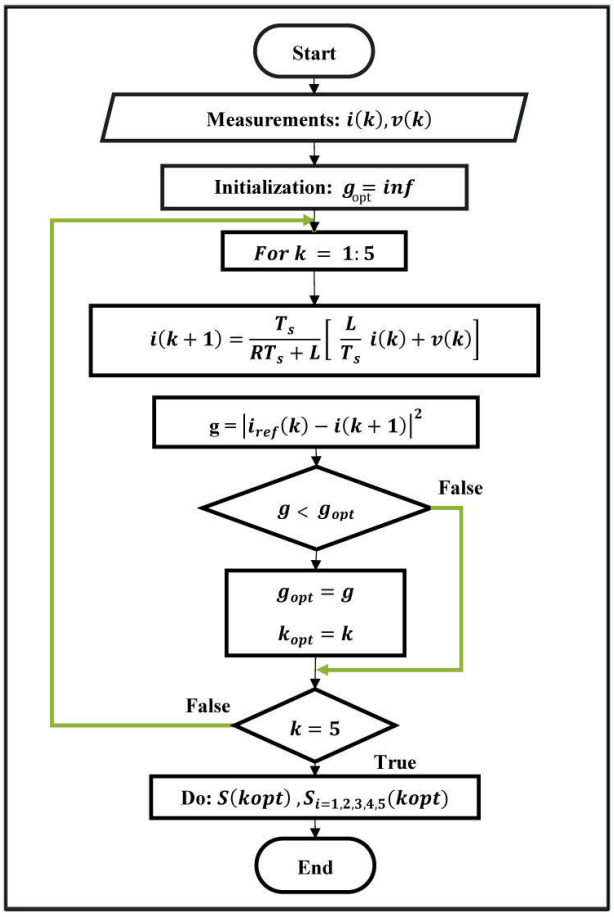


Figure 4.17 – Model predictive control MPC operation scheme. (click here to return to section 2.4.1)

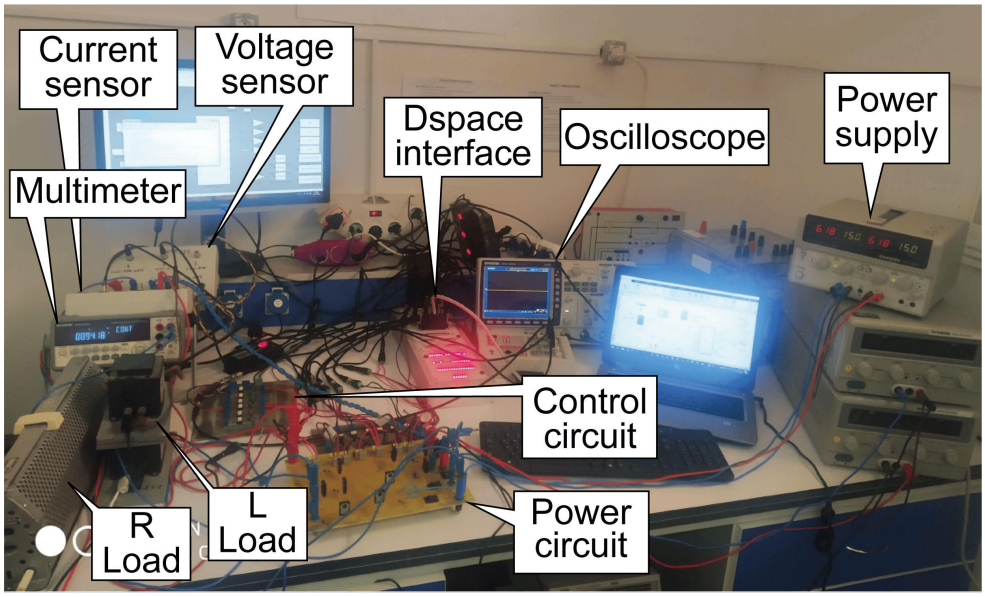


Figure 4.18 – Hardware setup of the implementation of WT-type inverter using control card Dscpace 1104

Table 4.9 – Experimental parameters of the practical system

Parameters	Values
DC voltage input	60 V
Reference current	4 A of magnitude
Resistor	12 Ω
Inductance	6 mH
frequency	50 Hz
Sampling time Ts	1e-4
IGBT reference	FGH 60N20

4.4 Results and interpretation

A prototype of a single-phase 3-level WT-type multilevel inverter was built at the LGEA laboratory, Figure 4.18, and Figure 4.20. The references of the components used to design the PCB board are organized in table 4.9. The Realtime hardware control used in the present validation is Dspace 1104. The sampling time is adapted to 100 μs.

Table 4.10 – Components parameters used in the practical experiment

Parameters	Values
Signal rising-edge	5 V
Optocoupler TLP 250 input	5 V
Optocoupler TLP 250 output	15V
IGBT FGH 60N20 V_{ds}	600 V
IGBT FGH 60N20 i_{ds}	20 A
IGBT FGH 60N20 V_{ge}	4 - 20 V
Control circuit resistors	100 Ω , 5 kΩ
Control circuit capacitors	22 µF

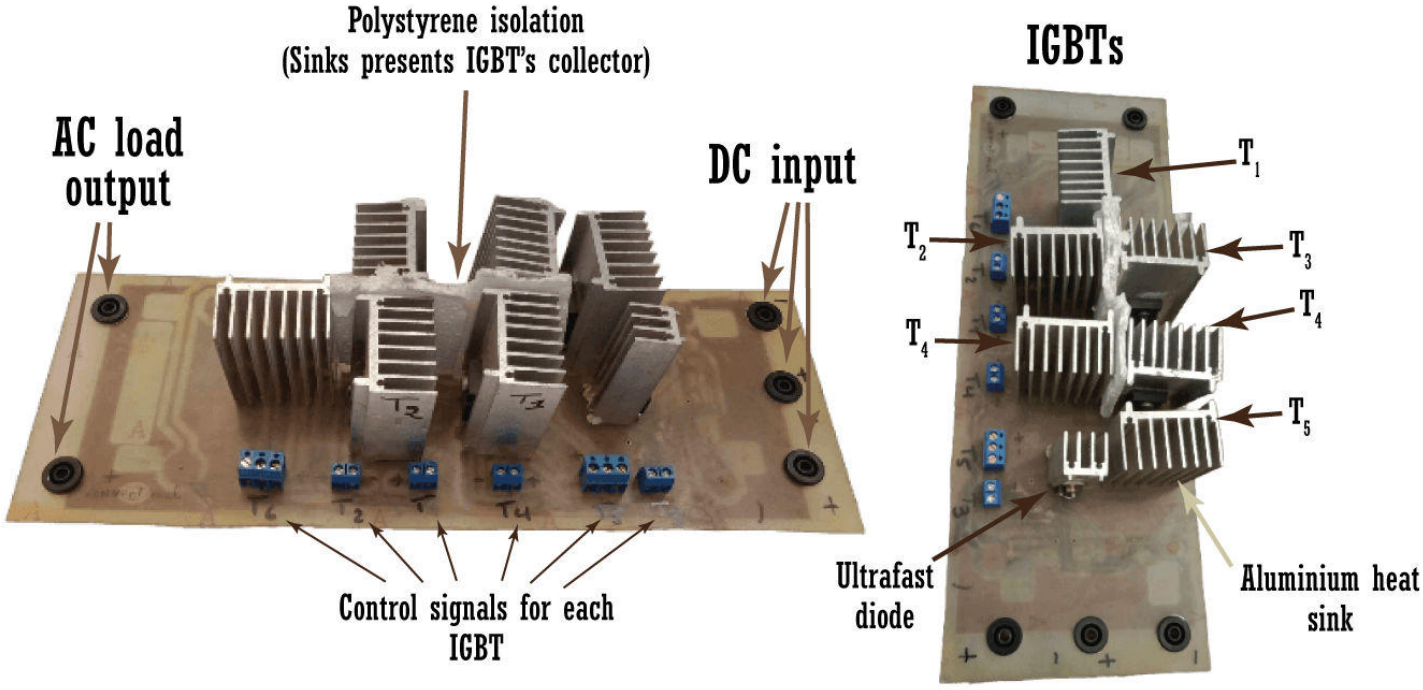


Figure 4.19 – A close look on the power circuit of the experiment

In this workbench, we built a control and power circuit using various components that suite the following operation:

• At each sampling time, the control signals of the IGBTs of the inverter are obtained from Simulink and issued from the digital output of the Dpace interface board IO3, I09, I07, ... etc.

• The characteristics of these signals are 5V for a rising edge and 0V for a falling edge.

• Therefore, the optic isolation of the optocoupler IC has to withstand the 5v rising edge and needs to be able to handle the operation frequency, that is the speed of variation of the signal.

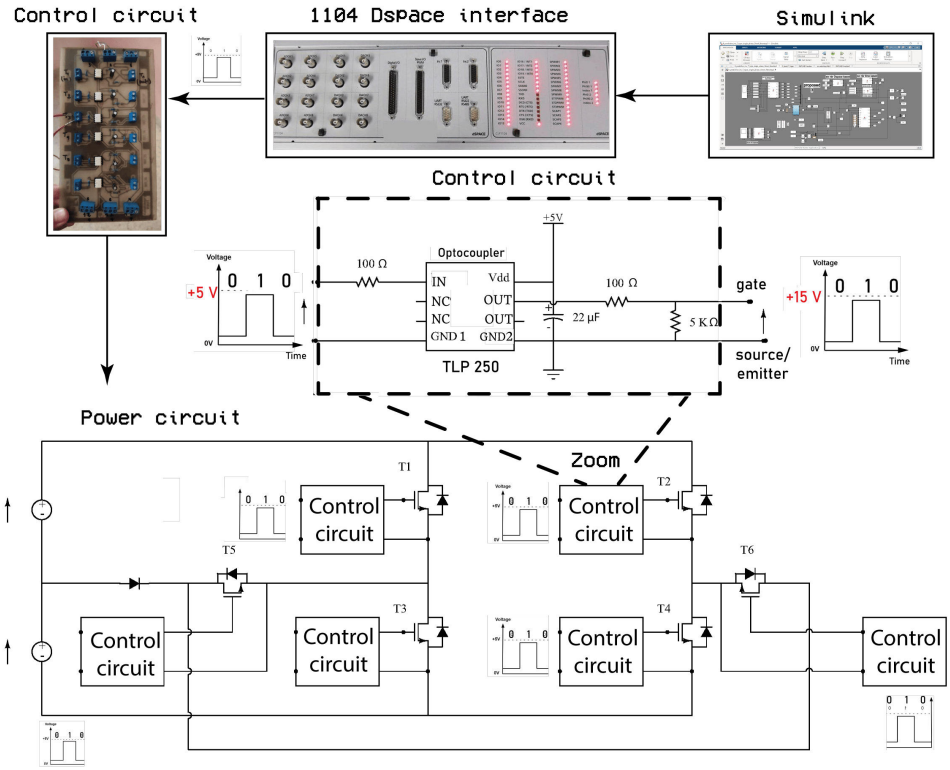


Figure 4.20 – synoptic scheme of the power and control circuit boards of the experiment

• Furthermore, The optocoupler has to provide an output high enough to close and open the gate of the IGBT. The previously stated requirements can be organized in table 4.10.

To evaluate the WT-type multilevel inverter we compare it to the mother topology T-type multilevel inverter. Therefore, we designed a 3-level classic T-type multilevel inverter PCB board for better assessment. The two inverters supply identical RL loads, are controlled with the same technique FS-MPC and use the same sampling time of 100 μs. The current reference for both inverters is a sinus curve of the same magnitude and they have the same DC input value.

Figure 4.21 shows the results of the two multilevel inverters. The left-hand figures represent the results WT-type inverter, while the right-hand results refer to the classical T-type inverter. The output voltage THD of the WT-type inverter is (39.42%) which is lower than the classical THD voltage (43.35%). Likewise, with the current, the FFT tool showed that the THD current is (3.83%) in the proposed inverter which is lower than the classical one (4.13%).

Figure 4.22 and Figure 4.23 present the number of switching of each switch, which includes turn-on and turn-off states. For diodes, we only count turn-off transition because the turn-on state does not induce losses [36]. The switching frequency is a very good

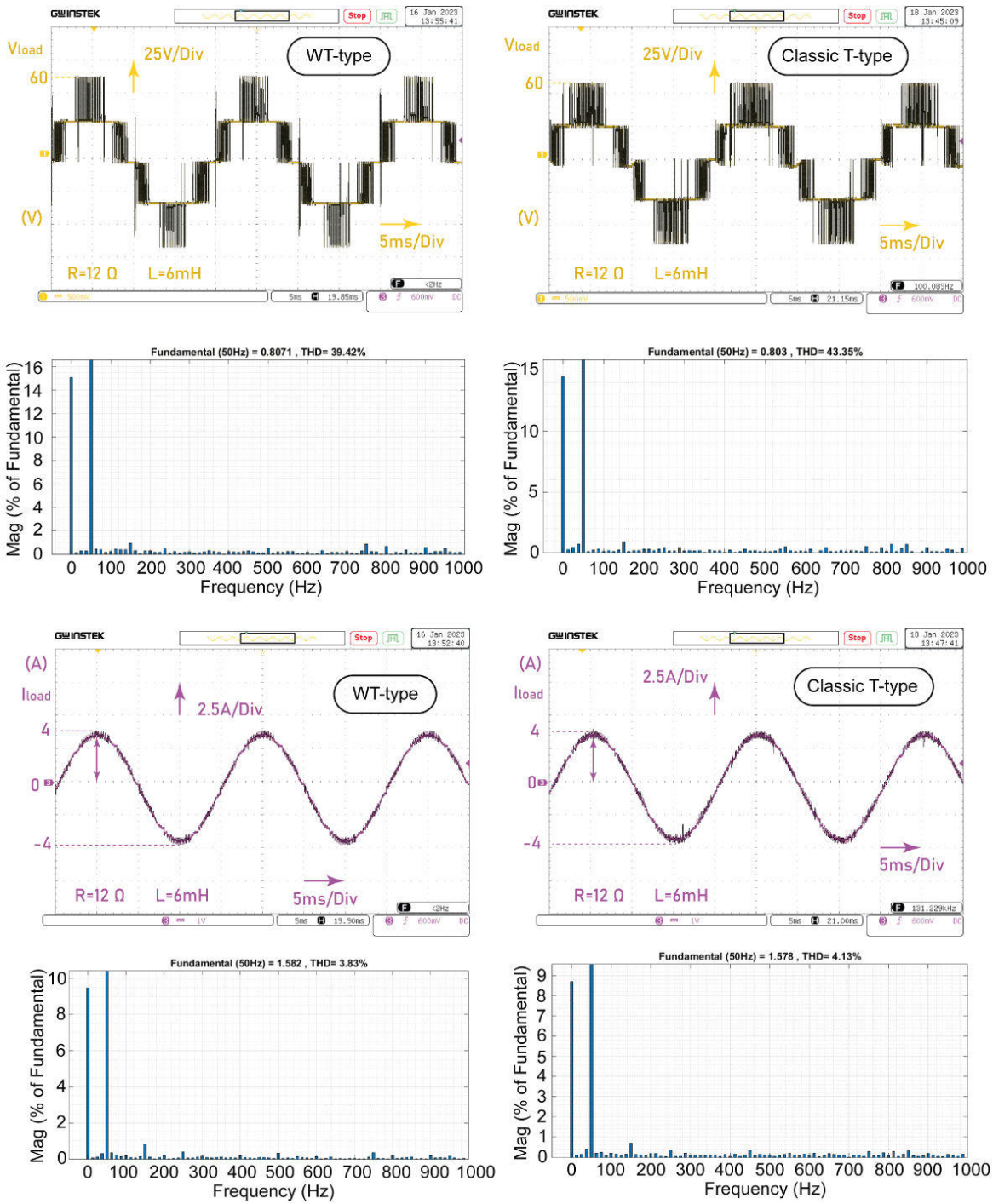


Figure 4.21 – The experimental results on the left-hand concerns the proposed inverter and on right-hand T-type where: Load voltage(a)(b), output voltage THD (c)(d), load current (e)(f), load current for FFT analysis (g)(h), harmonics content of current load (i)(j).

indicator of the switching losses and how the heat stress is distributed.

The switching frequency is calculated for each period of 0.02s and is obtained with the help of the ControlDesk platform. Figure 4.22 shows that the switching numbers of the WT-type components are very close. The maximum switching number is 44 and the lowest is 12, while the total number is 174. For the classical T-type in Figure 4.23 there is a large difference among the number of switchings, where the highest switching number is 90 and the lowest is 22 whilst the total switching number is 336.

Figure 4.24a and 4.24b are a colour presentation that shows heat distributions of WT-type and T-type multilevel inverters respectively during 4 periods. The number of switchings is used as an indicator of the heat. Each square refers to a switch as it is placed in the circuit of the inverter. The colour contrast refers to the intensity of heat such that The more the colour is dark the more heat there is.

For the classical inverter Figure 4.24b, heat is focused on the auxiliary circuit where the range between the highest switching number (T_5) and lowest (T_2) is (468-118) 350. This latter indicates that the heat is not homogeneous and is focused on parts over others. Whereas, in 4.24a, the colour contrast is similar for all parts of the WT-type multilevel inverter, furthermore, the intensity of colours is low which means that all parts operate with low heat. Also, we notice that the switchings range between the highest and lowest switch is only (226-78) 148. This means there is a balance in the distribution and the heat is homogeneously distributed over all parts. in addition, the parts of this inverter dissipate less heat than the classic one. The total switching number of the classic T-type multilevel inverter is 336, whilst the WT-type has only 174. Therefore, the WT-type is 2 times better in heat dissipation than the classical T-type.

Heat is an important parameter that assesses the reliability of the inverter. It reveals which parts have an extra burden over others, that is to say, which parts are likely to have a lower lifespan and, hence, lower capability of working under harsh climate conditions. On the other hand, a homogeneous heat distribution means a lower rate of failure and hence fitting working in remote places with a high repairs cost like offshore renewable systems and space. In addition, lower dissipated heat means a smaller cooling system, lower losses and thus lower cost.

Figure 4.25 presents the load THD current (a), output THD voltage (b), and a 3-D presentation of (a) and (b). The curves are obtained by setting the reference current to a certain value and measuring the current and voltage THD. This process is repeated for more than 45 different values of the reference current in the experimental bench. Figure 4.25a shows that the lowest THD recorded is 2.4% at i_{ref}=5.3A amplitude, this value increases the more we go away from the nominal point to reach 15% at i_{ref}=0.5A

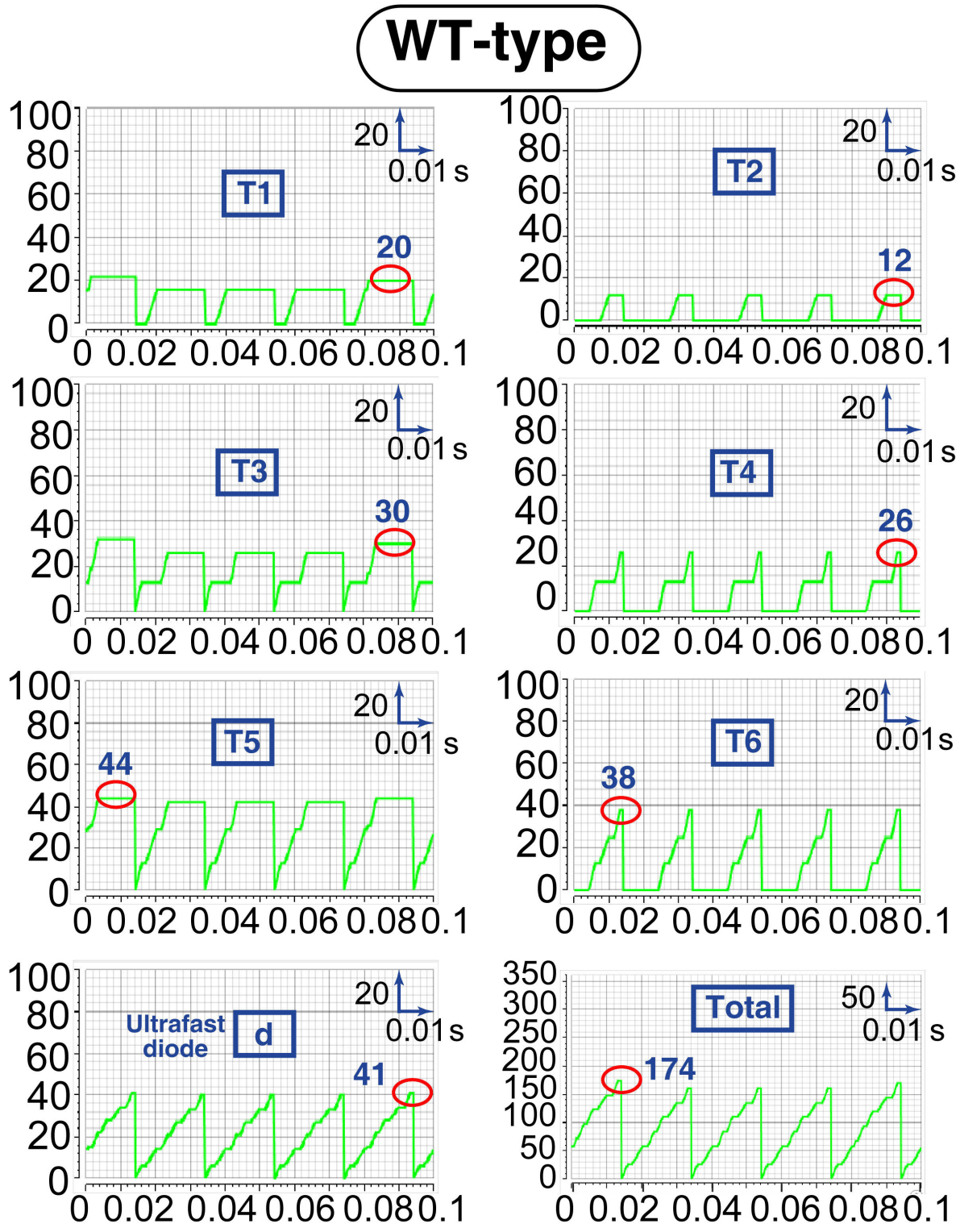


Figure 4.22 – Experimental number of switching performed by the IGBTs and ultrafast diode over 5 periods

amplitude. Figure 4.25b showed that the voltage THD decreases the more we approach

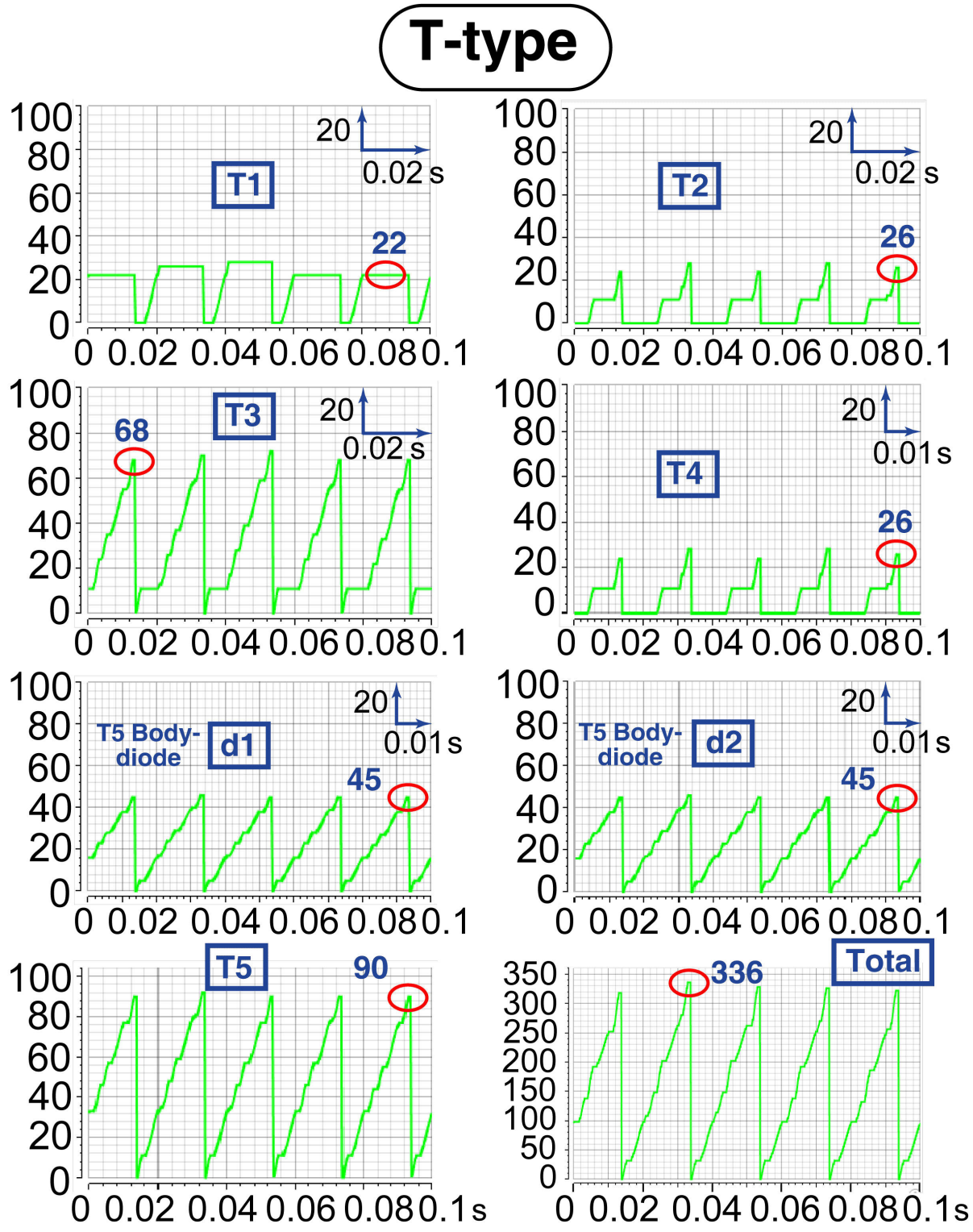


Figure 4.23 – Experimental number of switching performed by the IGBTs and body-diodes during 5 periods

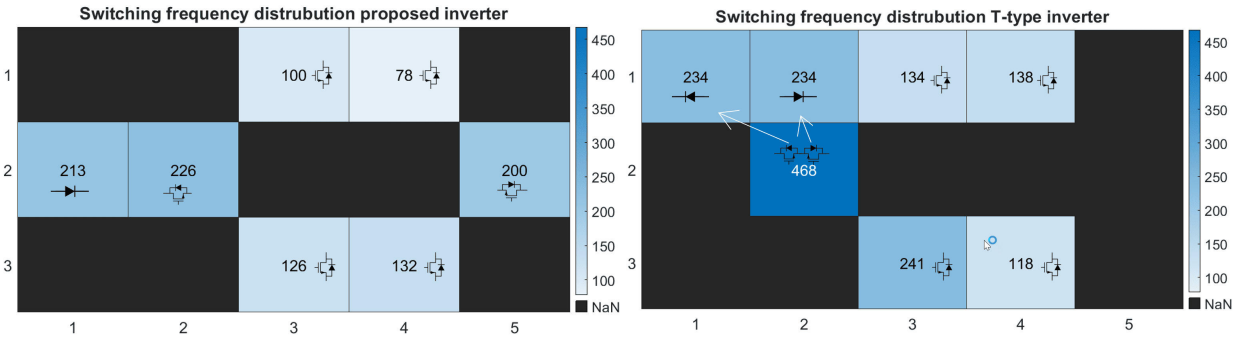


Figure 4.24 – Experimental heat distributions of: WT-type (a), classic T-type (b).

from the nominal point to reach the lowest value of around 23%.

Figure 4.26, Figure 4.27 and Figure 4.28 present the results of robustness tests using the FS-MPC algorithm. This latter is dependent on the value of the load R and L. In the first and second tests, we change the load resistor in the manipulation circuit from R=12 Ω to R=8.5 Ω then from R=12 Ω to R=15.3 Ω. This change is on the level of the power circuit while it is kept R=12 Ω in the algorithm's parameters. In the last test of Figure 4.28, we create a sudden change in the current reference with a large value: from 4.8A peak to 2.5A peak for 3 periods and returning to 4.8A peak again.

In the first test of Figure 4.26, before changing the load, the inverter operates in normal mode. After changing the load from 12Ω to 8.5Ω at instant t= 1.32s, the load current still follows the reference with a little more fluctuation. The load voltage level appears correctly with a little change in its pattern as shown in Figure 4.26. In the second test, Figure 4.27 the inverter is in normal operation, at instant t=2.885s, a change of the resistor from 12Ω to 15.3Ω, we notice that the load current still tracks the reference with very little fluctuations. For the voltage, we notice that the output voltage curve changes the pattern but still show the correct levels.

Figure 4.27 shows the results of the third robustness test in which the load resistor remains unchanged at R=12 Ω while the reference current is changed from the nominal value 4.8 A peak to 2.5 A and then restored to 4.8 A peak. Results show that after changing the reference at t=0.8s, the load current perfectly follows the reference with a very good transition state. After the current returns to the initial reference at t=0.86s the current still follows in a good tracking quality. During the steady states of the three cases, the current tracks the reference in a very good manner.

The robustness tests of the FS-MPC control applied to the WT-Type, showed that this control technique enjoys a highly robust parameters nperformance.

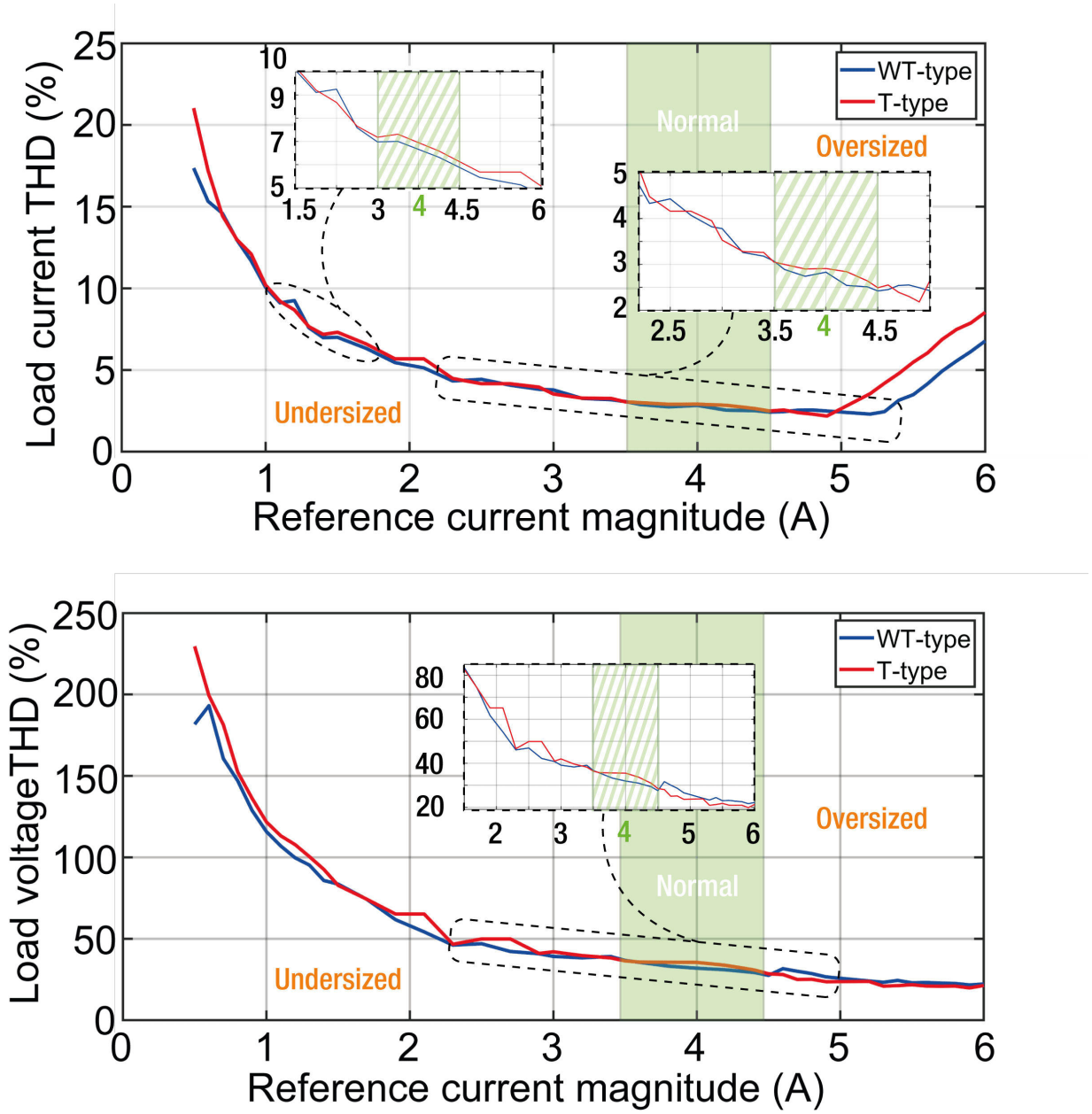


Figure 4.25 – Experimental load current THD versus reference current (a), Load voltage THD versus reference current (b).

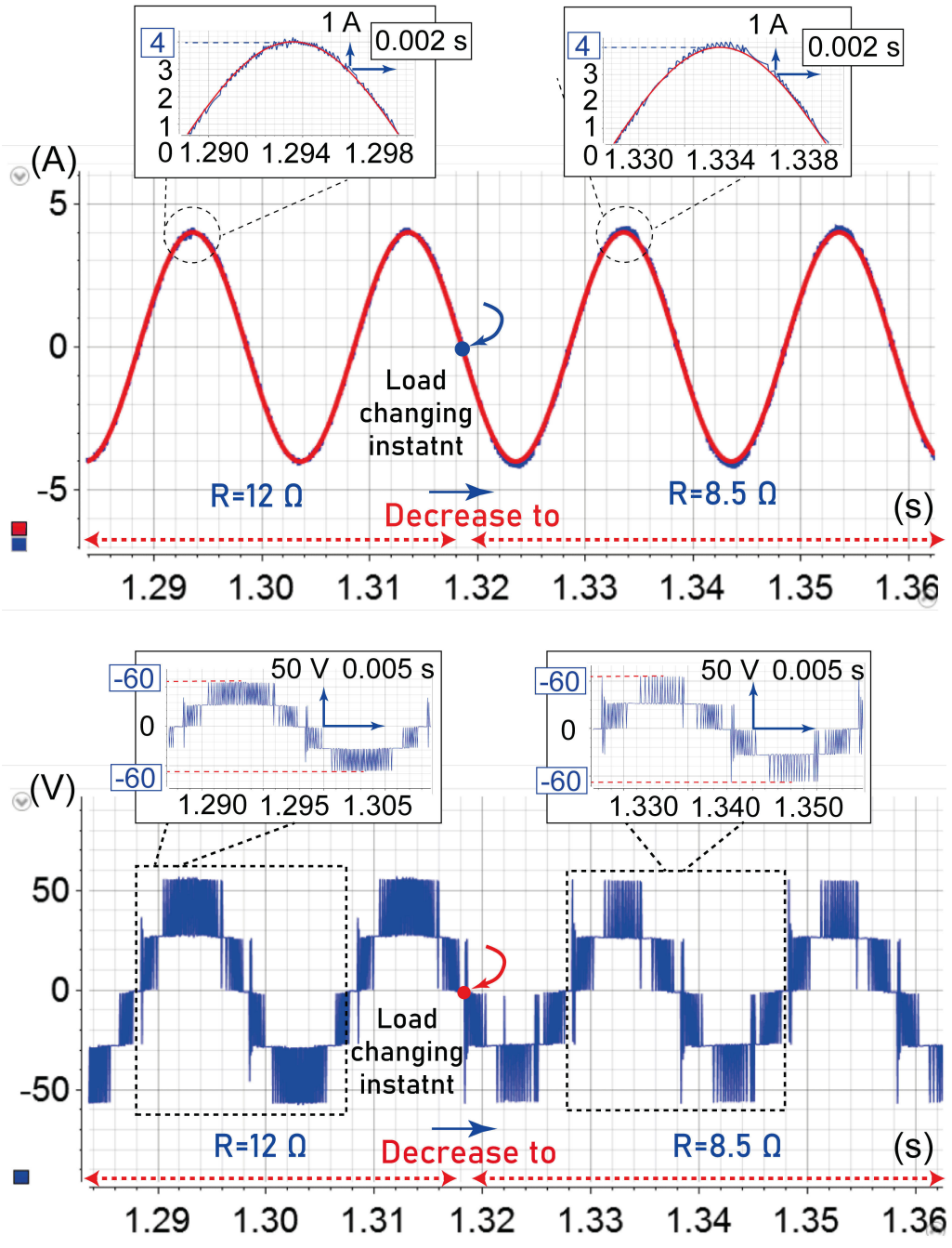


Figure 4.26 – Experimental robustness test: change of load R=12 Ω towards R=8.5 Ω.

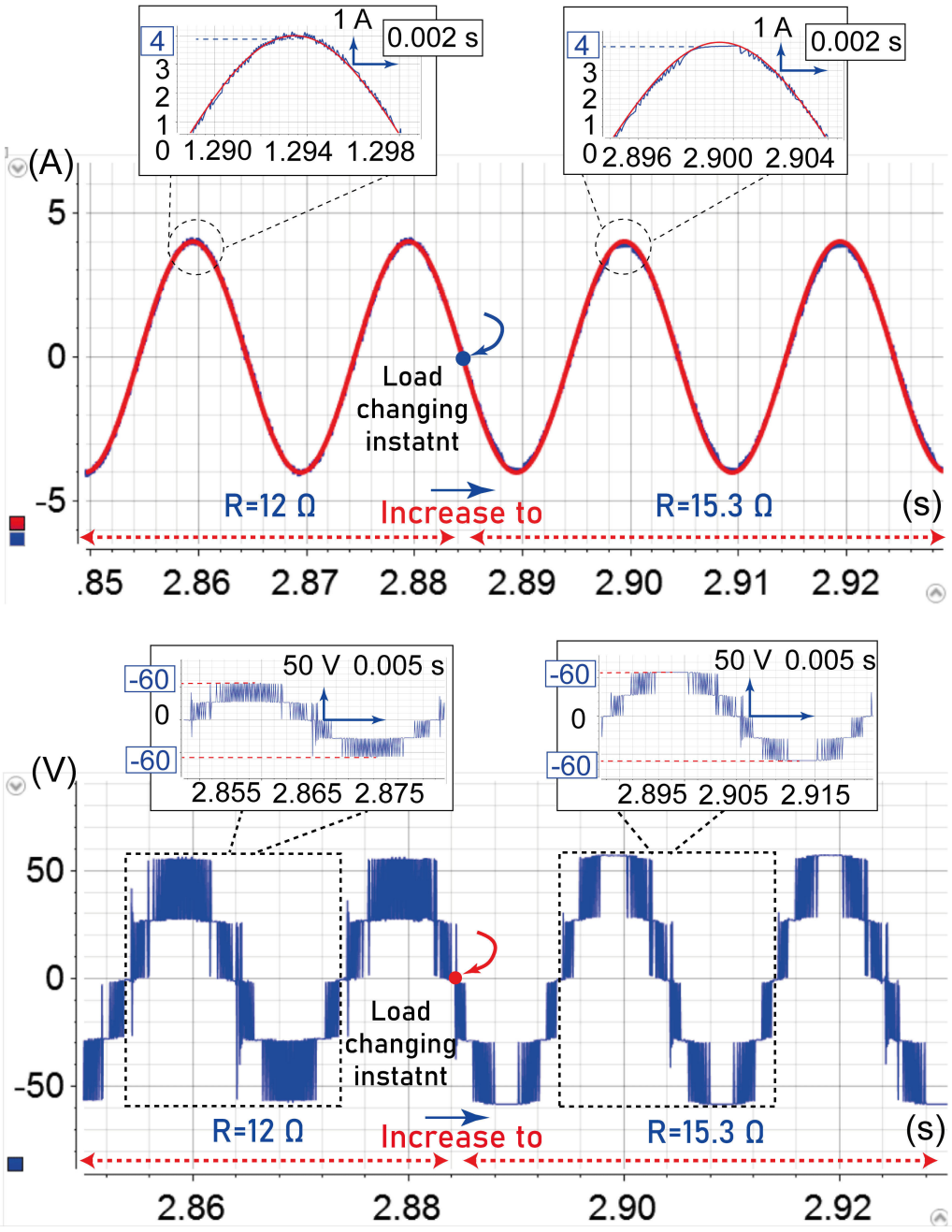


Figure 4.27 – Experimental robustness test: change of load R=12 Ω towards R=15.3 Ω

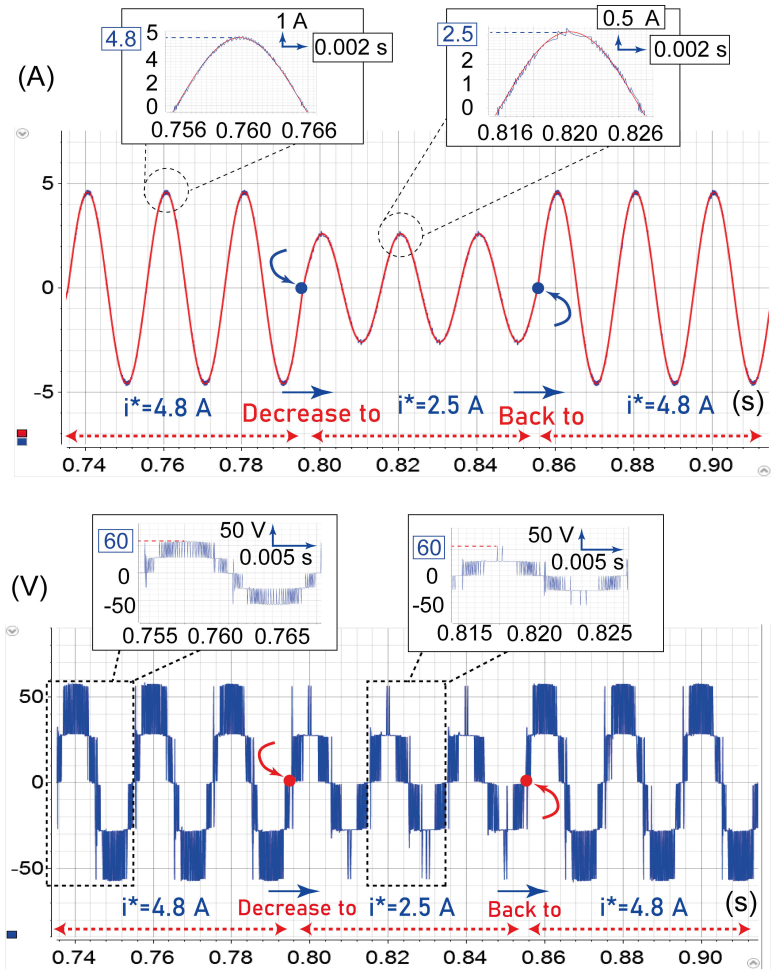


Figure 4.28 – Experimental robustness test: change of reference current 4.8A to 2.5A peak

4.5 Conclusion

This chapter introduced a state-of-the-art T-type multilevel inverter family where we started by showing the 2 radical forms of classical T-type multilevel inverter, then this analysis extended to include a wide range of multilevel inverters, which were analysed in detail showing their features and characteristics. These inverters are depicted on a timescale starting from 2014 up to now (2023). In the next section, we proposed a multilevel inverter extracted from a classical T-type called WT-type multilevel inverter. This inverter is in-depth studied by walking through the stages of optimisation step by step. The proposed inverter has the goal of reducing the switch count, enhancing the efficiency and making the inverter more cost-efficient. The studied multilevel inverter is evaluated on many aspects, for instance, device count compared to other topologies, cost compared to the classic T-type, heat stresses, conduction losses, and manufacturing design. In the last section, we applied the FS-MPC control technique to practically validate the performance of the WT-type with a 60v DC input and RL load of $R = 12$

and L= 12mH. Also, The performance of the studied inverter is compared to the classic T-type under the same conditions. Results showed that the current and voltage THD were lower in the WT-type. Also, we calculated the total number of switchings performed in 5 periods of operation and we deduced that the WT-type showed excellent thermal stress and a very low switching number which gave him the advantage of fitting working under extreme climate conditions and remote places like space and offshore plants. Finally, three robustness tests of the control technique were conducted: increase of the R, decrease of the R, and change of the reference current. After these tests, the inverter maintained a quality operation throughout all the tests.

In light of these results, the WT-type inverter showed very promising characteristics as it met all the optimisation objectives. Therefore, we can confidently say that the proposed inverter is a strong candidate for applications that require high reliability such as offshore plants, and space applications.

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Conclusion

Conclusion

The main objective of this dissertation has been to develop a static multilevel inverter for grid-connected renewable energy systems. Also, to develop a strategy of control that maintains the operation of the system uninterrupted while preserving the quality of the generated power.

In the first chapter, we carried out a review of renewable energy sources and the various fields of science they attracted. We presented the various forms of renewable energy with strong potential to become a primary source in the next decades. We also showed the motivations and factors that make renewable energy an attractive option such as the cheap cost and its availability in all countries. We also presented a country with exceptional renewable energy deposits: Algeria. We also discussed the shy state of solar potential in this country along with the various projects installed. In the second section, we tackled a brief history of the invention and emergence of PV cells. we also presented the structures of PV systems and their development over time. Furthermore, we explained the general structure of PV systems which includes the parts: dc-dc choppers, dc-ac inverter and load/grid. The last section of this chapter dealt with very important basics and concepts that help understand and asses renewable energy systems.

Chapter 2 gave special attention to the dc-ac part of the PV system. This Chapter started with a state-of-the-art of a famous family of Multilevel inverters. The characteristics of the classical multilevel inverters were analysed stating their pros and cons. Various types of emergent multilevel inverters were also included and studied individually by showing their features and operation principles. In the second section, The two families of control PWM and MPC with their various techniques were presented. In the last section, all the studied topologies were simulated using FS-MPC and compared under the same parameters. In terms of the THD content in the load current, results showed that the classical topologies struggle in higher levels due to their cumbersome circuit. Also, emergent topologies provided a current with lower THD with relatively simpler circuits.

In light of the structures presented in Chapter 1, Chapter 3 introduced a study of a typical PV grid-connected system. This system contained: a dc-dc chopper that guarantees a maximum power extraction using an MPPT, a 9-level T-type multilevel inverter and a grid. The PV system was controlled using FS-MPC, which controlled the chopper and inverter with one algorithm. Section two of this Chapter treats a state of operation under failure. In this context, a proposed algorithm based on IFS-MPC was implemented to surpass these faults while preserving a continuous operation of the system, respecting the IEEE quality standards without additional components or intervention on the power circuit level. The results showed that the algorithm tolerated the failures with an excellent transient state.

Chapter 4 aimed to propose a topology called WT-type derived from the classical T-type multilevel inverter. This chapter started with an extensive state of the art of T-type multilevel inverters, in which various types were analysed and discussed. All these multilevel inverters were organised on a timescale to facilitate tracking the development of converters of this family over time. In section two, the steps of development of the classical T-type are detailed and illustrated. In addition, the core features of the resultant inverter (WT-type inverter) were investigated and interpreted through experimental validation. Results showed an advantage of the proposed inverter over the classical inverter on many levels: the current and voltage THD content, heat stress, reliability and efficiency. WT-type multilevel inverter enjoys also lower switching and conduction losses and hence lower volume of the cooling system.

These results show that the proposed work matches the goals set at the start of the dissertation.

future work

The time framework of this thesis was limited which prevented the inclusion of many additional aspects to this work, for instance: the practical validation of the fault-tolerant algorithm is presented in Chapter 3. The work consists of building the PCB circuit of a 9-level classical T-type multilevel. Auxiliary circuits are also needed for the induction of multiple failure scenarios in real-time while preserving the safety of the circuit's components. DC-link voltage capacitors have to withstand at least the total input voltage vdc so they handle the case of unbalance or dysfunction of the algorithm. Figure 4.29 and Figure 4.30 below shows the uncompleted test bench for this Chapter.

Another aspect that deserves attention is the tuning of weighting factors of the cost function of the FS-MPC. In the present work, the weighting factors were determined by

an empirical method, where in the simulation we intuitively try and see various values and finally choose one. This method does not give the absolute optimum values to our system, therefore, using techniques like AI could greatly help to improve the procedure.

One other fertile field is cyber security in renewable power systems. With the emergent role of microgrids in building future smart cities, it showed an increasing dependency on information and communication technologies. This dependency created vulnerabilities that present a real threat to the proper operation of the system and the safety of millions of people. It includes for instance the detection and identification of the misleading signals issued from the sensors used for control.

Publications

During the course of this dissertation, a journal paper was published in Power Electronics and Drives, rehearsing the work introduced in Chapter 3. Also, a second journal paper is ready to be submitted about the subject introduced in chapter 4 which will be about *"A-wings T-type (WT-type) multilevel inverter with reduced cost and enhanced efficiency"* :

— Wassim Boudja and Kamel Barra. Integrated model predictive control of a single-phase multilevel t-type converter for a photovoltaic grid-connected system under failure conditions. Power Electronics and Drives, 8(1):142–164, 2023

This work led also to two publications in international IEEE conferences in the ICSRESA 2019, and ICAEE 2023 :

— W Boudja, K Barra, SEI Remache, S Mekhilef, and P Wira. Optimized t-type multilevel converter under finite set model predictive control. In 2022 2nd International Conference on Advanced Electrical Engineering (ICAEE), pages 1–6. IEEE, 2022.

— Wassim Boudja and Kamel Barra. A comparative study of multilevel topologies using finite set model predictive control. In 2019 1st International Conference on Sustainable Renewable Energy Systems and Applications (ICSRESA), pages 1–8. IEEE, 2019

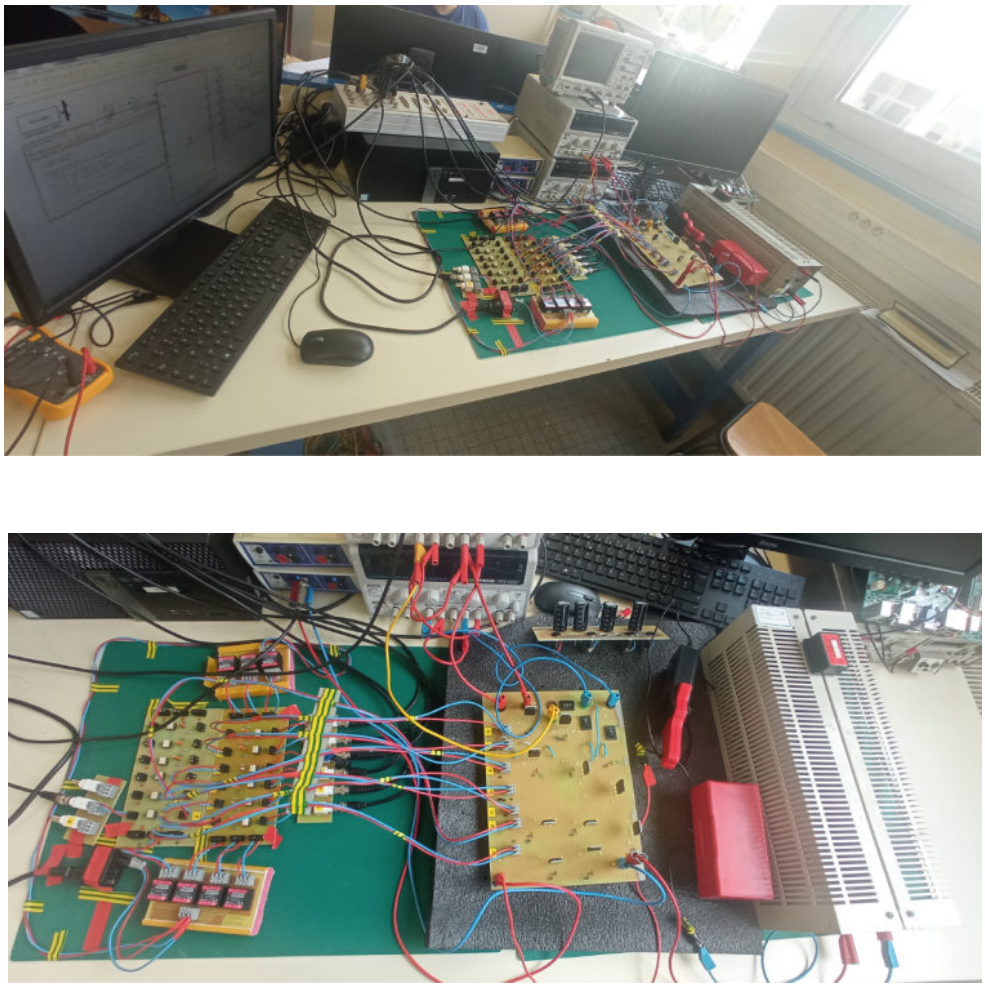

Figure 4.29 – Experimental validation of the fault-tolerant FS-MPC based proposed algorithm

Figure 4.30 – 9-level healthy output Voltage: incomplete results from the validation of the fault-tolerant FS-MPC based algorithm