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Numerical Study and Performance Analysis of Carbone Nanotube Field Effect Transistors

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Abstract - As transistors are scaled down to nanometers, the theory and structure of nanometers devices such as carbon nanotubes field effect transistors (CNTFET) are being extensively studied. Self consistent solution of the Poisson and Schrödinger equations is performed using the non-equilibrium Green's function (NEGF) formalism to investigate the impact of nanotube diameter, gate oxide thickness and high-k gate dielectric permittivity parameters on the coaxially gate, n-type CNTFET. Our results show that the nanotube diameter and gate oxide thickness influences the ION/IOFF current ratio, the drain induced barrier lowering (DIBL), the subthreshold slop as well as transconductance and drain conductance. Furthermore, in this work we focus on the impact of high-k gate dielectric permittivity on the performance of CNTFETs. Using high-k dielectric is caused by the enhancement in device characteristics. A good agreement with numerical simulation results is obtained.

I. INTRODUCTION

The carbon nanotube field effect transistor (CNTFET) is a promising device to supersede the MOSFET at the end of the technology roadmap of CMOS [1-4]. Since the first reports of single-walled carbon nanotubes (CNTs) in 1993 [5], they have been the subject of intense interest for basic and applied research. In CNTFETs, ballistic or near-ballistic transport phenomena have been observed [7-9], and the existing design infrastructure and fabrication process of CMOS-based MOSFETs can be also used for CNTFETs [10–12].

Rapid progress in the field has recently made it possible to fabricate digital and analogue CNTFET bases circuits, such as logic gate, static memory cells [13-14]. A CNTFET with a short gate width is expected to have marked advantages in terms of operational frequency and will be a subject of future studies.

We present in this paper, a scaling study of carbon nanotube field-effect transistors (CNTFETs). We investigate the scaling issues in device performance focusing on I_{ON}/I_{OFF} current ratio, the drain induced barrier lowering (DIBL), subthreshold slope as well as transconductance and drain conductance with different carbon nanotube (CNT) diameters and gate oxide thicknesses.

Silicon dioxide (SiO_2) has facing the scaling limitation due to direct tunneling current that limits low power application and reliability problem. Recently, many high-k materials such as HfO_2 (k=16), ZrO_2 (k=25), Ta_2O_5 (k=50) and TiO_2 (k≈35-100) [15-19] have been introduced as alternative gate dielectrics to overcome leakage current problem. To consider the benefits of both high-k dielectrics and CNTFETs, in this paper we present also the effects of high-k gate dielectric on the performances of CNTFETs. We have simulated the structure using a two-dimensional (2-D) quantum simulation.

II. DEVICE STRUCTURE

The modeled device, a coaxially gate, n-type CNTFET is schematically shown in Fig. 1(a) and 1(b). The nanotube length is 50 nm, consisting of ~1.2×10^4 carbon atoms. The intrinsic channel length is 20 nm, and the doped source/drain length is 15 nm.

To simulate the comportment of a CNTFET, the following model is used at different nanotube diameters, gate oxide thicknesses and high-k gate dielectric constants.

The chiralities of the CNTs used are (13,0), (16,0), (19,0), (23,0), (25,0). The gate oxide thicknesses (tox) used are 1.5 nm, 3 nm, 4.5 nm, 6 nm and 7 nm. In addition the gate dielectric constants are 3.9, 16, 25, 50, and 80. These dielectric constants correspond to the dielectric constants reported for SiO_2, HfO_2, ZrO_2, Ta_2O_5, and TiO_2, respectively.

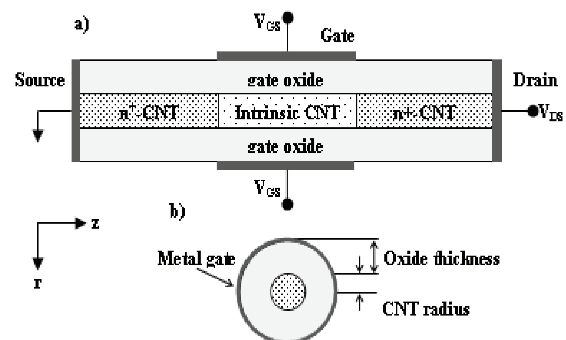

Figure 1. Schematic diagrams of the modeled, coaxially CNTFET

III. MODELING AND SIMULATION

In order to simulate the proposed devices [20], self consistent solution of the Poisson and Schrödinger equations has been performed within the NEGF formalism with a mode space approach, developed in [21-22], Poisson equation is written as:

$$\nabla^2 V(r,z) = \frac{-q}{\varepsilon}[p - n + N_D^+ + N_A^- + n_T] \quad (1)$$

The electron and hole concentrations are computed by solving the Schrödinger equation.The electron density is computed from the density of states (DOS), derived by the NEGF formalism. It can be calculated as follows:

$$n = \int_{Ei}^{+\infty}[D_S f(E - E_{FS}) + D_D f(E - E_{FD})]dE \quad (2)$$

Once, self consistency is achieved, the source-drain current can be expressed as:

$$I = \frac{4q}{h}\int \quad T(E)[f(E - E_{FS}) - f(E - E_{FD})]dE \quad (3)$$

IV. SIMULATION RESULTS

A. Effect of nanotube diametre

The nanotube diameter is varied from 1 nm, corresponding to the chirality vector of (13,0), to about 2 nm, corresponding to chirality vector of (25,0). While the gate oxide thickness is fixed at 1.5 nm and high-k gate dielectric is fixed at k=16. The I_{ON}/I_{OFF} current ratio of the CNTFET for different chirality vectors, i.e. different diameters of the zigzag CNT, is depicted in Fig. 2. I_{ON} is obtained at V_{GS} = 1 V and V_{DS} = 1 V, I_{OFF} is determined as the current obtained for V_{GS} = 0 V and V_{DS} = 1 V. As shown in Fig. 2, I_{ON}/I_{OFF} current ratio is improved with increase in the nanotube diameter. This comes from the correlation of the band-structure with the CNT diameter. Using a larger diameter reduces the bandgap, therefore both the ON-current and the leakage current I_{OFF} increase, and I_{ON} increases rapidly.

Thus a significant increase of the I_{ON}/I_{OFF} current ratio is observed. Moreover, the I_{ON}/I_{OFF} current ratio is about 10^6 at a larger diameter, indicating that the CNTFETs have a good current switch capability. So this point must be carefully taken into consideration to achieve the suitable electrical characteristics.

For short channel devices, application of a high drain-to-source bias can shorten the threshold voltage and increase the off-currents. This is known as drain induced barrier lowering (DIBL). In CNTFETs, the DIBL effect is still a primitive problem and open for further study [23]. Fig. 3 shows the effect of varying the nanotube diameter on the DIBL. The DIBL is accessed using the classical formula:

$$\text{DIBL} = \frac{V_{TH}(\text{low } V_{DS}) - V_{TH}(\text{high } V_{DS})}{\text{high } V_{DS} - \text{low } V_{DS}} \quad (4)$$

From the simulation results, it can be drawn that the DIBL is considerably improved with decreasing the nanotube diameter; therefore, the control of gate on the channel becomes stronger. One notes a reduction around 53% of DIBL when CNT chiralities varying from (13, 0) CNT to (25, 0) CNT.

Another important parameter is the subthreshold slope S that measures the how efficiently the gate controls conduction though the channel. It is defined as S = $\Delta V_{GS}/\Delta \log 10\ (I_{DS})$. In a transistor with ohmic source and drain contacts (as in a conventional Si MOSFET), S is limited by thermionic emission over the channel and is ~(kB T/ q)ln10. Thus, at room temperature, its limiting value is 60 mV/dec. A small subthreshold slope is desired for low threshold voltage and low-power operation for FETs scaled down to small size. Fig. 3 shows the simulated subthreshold slope as a function of the nanotube diameter. It can be observed that when the nanotube diameter decreases, S decreases slightly (practically remains constant around 67 mV/decade).

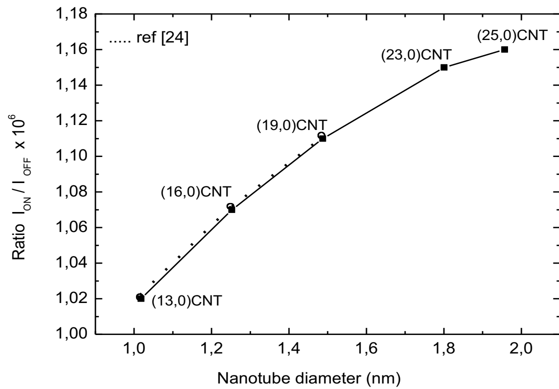

Figure 2. I_{ON}/I_{OFF} current ratio as a function of the nanotube diameter

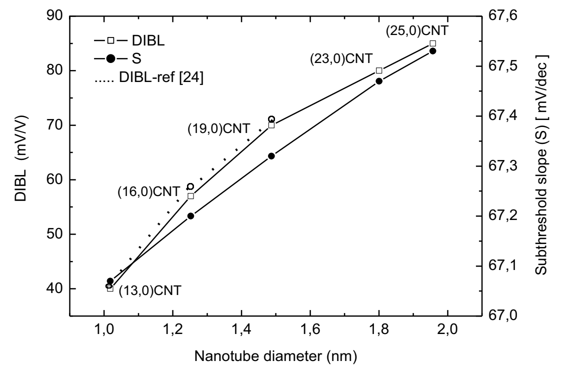

Figure 3. Drain induced barrier lowering (DIBL) and subthreshold slop versus nanotube diameter

The transconductance, an important device parameter, is defined as measure of device gain and is directly related to the circuit speed. The transconductance gm curve is obtained by differentiating the drain current I_{DS} with respect to the gate voltage V_{GS} at a given drain bias. $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$

As can be seen from Fig. 4, when the nanotube diameter increases, the transconductance gm increases. The drain conductance defined by $g_d = \frac{\partial I_{DS}}{\partial V_{DS}}$ is presented also in Fig. 4 for different values of nanotube diameter. It is observed that gd is higher for larger nanotube diameter. One notes a voltage gain gm/gd around ~25 whatever the value of nanotube diameter is. To check the accuracy of our numerical calculations, our results were compared with simulated results presented in ref [24] (dotted lines) .good agreement has been found in figures 2 and 3.

B. Effect of gate oxide thikcness

In this section, we investigate the effect of different gate oxide thickness (tox) on the CNTFET performance. Fig. 5 represents the evolution of I_{ON}/I_{OFF} current ratio with gate oxide thickness varying from 1.5 nm to 7 nm.

As shown in the figure, a larger gate oxide thickness lowers I_{ON}/I_{OFF}. This leads to reduce the control of the gate over the channel region.

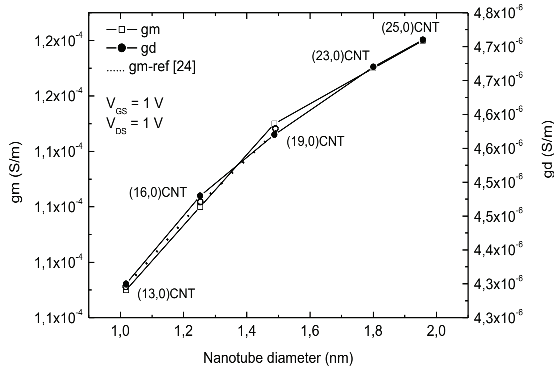

Figure 4. Variation of gm and gd as a function of nanotube diameter

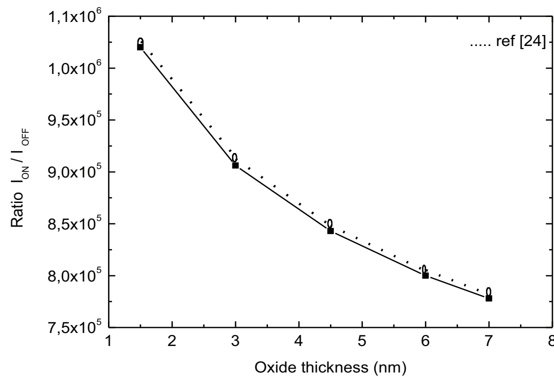

Figure 5. I_{ON} /I_{OFF} current ratio as a function of the oxide thickness.

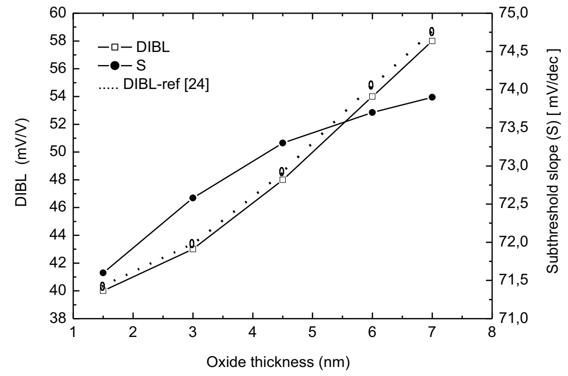

Figure 6. Drain induced barrier lowering (DIBL) and subthreshold slop versus oxide thickness

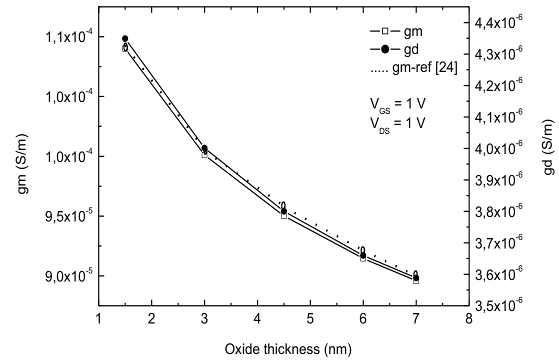

Figure 7. Variation of gm and gd as a function of oxide thickness.

The DIBL is calculated as a function of gate oxide thickness. This is illustrated in Fig. 6, an important reduction in DIBL around 30 % can be observed when tox changes from 7 nm down to 1.5 nm.

The effect of gate oxide thickness on transconductance gm and drain conductance, gd, is shown in Fig. 7. A larger gate oxide thickness leads to a smaller gd and gm. We can conclude that the variation of the gate oxide thickness has a larger effect because it determines the controllability of the gate over the channel region. Our results were compared with simulated results presented in ref [24] (dotted lines) .good agreement has been found in figures 4-7.

C. Effect of high –k gate dielectric permettivity

In this section, to highlight our analysis, we varying the gate dielectric permittivity from 3,9 to 80. Fig. 8 shows the evolution of I_{ON}/I_{OFF} current ratio as function of the gate dielectric permittivity (k). It can be seen from the figure that with increasing k the I_{ON}/I_{OFF} current ratio increases ($\geq 10^4$ is typically desirable in logic applications) and leads to efficient gate switching.

The DIBL and subthreshold slope (S) are calculated as a function of gate dielectric permittivity (k). These are illustrated in Fig. 9. As seen in this figure, the DIBL and subthreshold slope improve with increasing k and the control of gate on the channel becomes stronger. One notes a considerable reduction of DIBL from 180 mV/V to

about 20 mV/V when gate dielectric permittivity increases.

As shown in Fig. 10, it is seen that as gate dielectric permittivity increases the transconductance gm and the drain conductance gd continues to increase. Consequently, voltage gain is higher for high-k gate dielectric. Noting that when the gate dielectric permittivity increases the CNTFET characteristics is not affected by the fringing-induced barrier lowering (FIBL). This is due to the coaxially CNTFET structure. Our results were compared with simulated results presented in ref [25] (dotted lines) .good agreement has been found in figures 8.

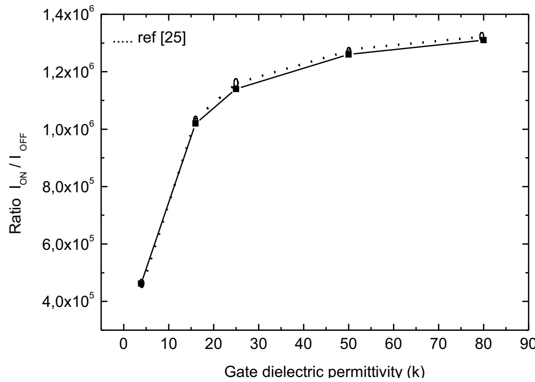

Figure 8. I_{ON} /I_{OFF} current ratio as a function of the gate dielectric permittivity.

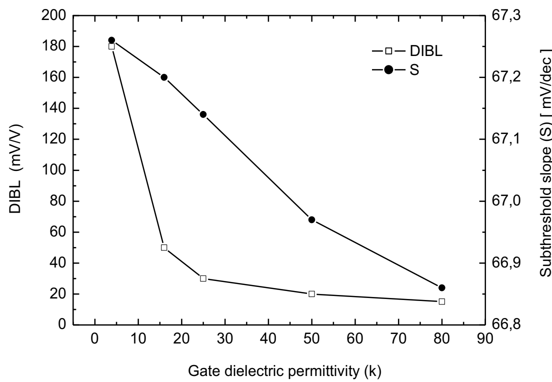

Figure 9. Drain induced barrier lowering (DIBL) and subthreshold slop versus gate dielectric permittivity.

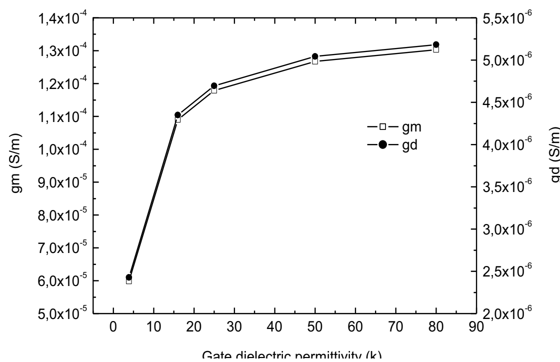

Figure 10. Variation of gm and gd as a function of the gate dielectric permittivity.

V. CONCLUSION

Based on the I_{ON}/I_{OFF} current ratio, drain induced barrier lowering (DIBL), subthreshold slope, transconductance and drain conductance variation the CNTFET behavior is evaluated. We concluded that using large CNT diameter and thinner gate oxide are caused by the enhancement in on-state current, transconductance and drain conductance. In addition, off-state current, DIBL and subthreshold slope improve in CNTFETs with thinner gate oxide, but they become worse in CNTFETs with large nanotube diameter.

Furthermore it is found that using high-k dielectric is caused by I_{ON}/I_{OFF} current ratio increases and leads to high on-state current. Also DIBL is significantly improved in high-k gate dielectric, on the other hand we found that the influence of high-k gate electric on subthreshold slope is slight. It is also found that using high-k gate dielectric in CNTFET is caused by the enhancement in transconductance and drain conductance, consequently, voltage gain is higher.

REFERENCES

[1] International Technology Roadmap for Semiconductors, http://public.itrs.net/.

[2] S. Tans, A. Verschueren, and C. Dekker, Nature., vol. 393, pp 49, 1998.

[3] H. J. Dai, A. Javey, E. Pop, D. Mann, and Y. Lu, NANO, vol. 1, pp. 1, 2006.

[4] Ph. Avouris, Phys. World, vol. 20, pp. 40, 2007.

[5] S. Iijima, and T. Ichihashi, "Single-shell carbon nanotubes of 1-nm diameter," Nature, vol. 363,pp. 603-605, 1993.

[6] S. J. Wind, J. Appenzeller, and P. Avouris, "Lateral scaling in carbon nanotube field-effect transistors," Phys. Rev. Lett, vol. 91, pp. 058–301, 2003.

[7] Y. Park, S. Rosenblatt, Y. Yaish, V. Sazonova, H. Ustunel, S. Brag, T. A. Arias, P.W. Brouwer, and P. L. McEuen, "Electron–phonon scattering in metallic single-walled carbon nanotubes," Nano Lett, vol. 4, pp. 517–520, 2004.

[8] W. Liang, M. Bockrath, D. Bozovic, J. H. Hafner, M. Tinkham, H. Park, and F. Perot, "Interference in a nanotube electron waveguide," Nature, vol. 411, pp. 665–669, 2001.

[9] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," IEEE Trans Electron Dev, pp. 703–706, 2004.

[10] H. Ohnaka, Y. Kojima, S. Kishimoto, Y. Ohno, and T. Mizutani, "Fabrication of carbon nanotube field effect transistors using plasma-enhanced chemical vapor deposition grown nanotubes," Jpn. J. Appl Phys, vol. 45, pp. 5485–5489, 2006.

[11] J. Li, Q. Zhang, Y. Yan, S. Li, and L. Chen, "Fabrication of carbon nanotube field-effect transistors by fluidic alignment technique," IEEE Trans Nanotechnol, vol. 6, pp. 481–484, 2007.

[12] V. Derycke, R. Martel, J. Appenzeller, and Ph Avouris, "Carbon nanotube inter-and intramolecular logic gates," Nano. Lett, vol. 9, pp. 453–456, 2001.

[13] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, "Logic circuits with carbon nanotube transistors," Science, vol. 294, pp. 1317–1320, 2001.

[14] J. L. Autran, R. Device, C. Chaneliere, and B. Balland, "Fabrication and characterization of Si-MOSFETs with PECVD amorphous Ta_2O_5 gate insulator," IEEE Electron Device Lett., vol. 18, pp. 447-449, Sept 1997.

[15] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Ki, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, "Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-AL2O3 gate dielectric," in IEDM Tech. Dig., pp. 645-648, 2000.

[16] R. Choi, K. Onishi, S. K. Chang, H. J. Cho, Y. H. Kim, S. Krishnan, M. S. Akbar, and J. C. Lee, "Effects of deuterium anneal on MOSFETs with HfO2 gate dielectrics," IEEE Electron Device Lett, vol. 24, pp. 144-146, Feb 2003.

[17] W. J. Qi, R. Nieh, B. H. Lee, K. Onishi, and L. Kang, "Performance of MOSFETs with ultrathin ZrO_2 and Zr silicate gate dielectrics," in IEEE Symp. VLSI Tech. Dig, pp. 15-16, 2000.

[18] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," J. Appl. Phys, vol. 89, No. 10, pp. 5243–5275, May 2001.

[19] J. Guo, S. Datta, MS. Lundstrom, and MP. Anantram, "Towards multiscale modeling of carbon nanotube transistors," Int J Mult Comp Eng,vol. 2, pp. 257–276, 2004.

[20] Liu Xinghui et al., " Study on transport characteristics of CNTFET based on NEGF theory," 2011 IEEE International Conference of Electron Devices and SolidState Circuits (EDSSC). 17-18 Nov. 2011

[21] J. Guo, S. Datta, MS. Lundstrom, and MP. Anantram, "Towards multiscale modeling of carbon nanotube transistors," Int J Mult Comp Eng,vol. 2, pp. 257–276, 2004.

[22] S. O. Koswatta, M. S. Lundstrom, M. P. Anantram, and D. E. Nikonov, "Simulation of phonon-assisted band-to-band tunneling in carbon nanotube field-effect transistors," Appl. Phys. Lett., 87, 253107, 2005.

[23] Z. Hailiang, S. Bingcai, C. Yaqing, Z. Minxuang, and H. Yue , "Numerical study of DIBL effect in Carbon Nanotube-FETs, Nanotechnology," IEEE. NANO 2009, 9th IEEE Conference on Publication, pp. 752–755, 2009.

[24] Z. Arefinia, A.A. Orouji, "Novel attributes in scaling issues of carbon nanotube field-effect transistors," microelectronics journal 40 (2009) 5-9.

[25] Z. Arefinia, A.A. Orouji, "Investigation of the novel attributes of a carbon nanotube FET with high-k gate dielectrics," Physica E: Low-dimensional Syst. Nanostructures 40 (2008) 3068–3071.