A Low-Power and High Sensibility of the Smart CMOS(Si and 4H-SiC) Temperature Sensor in 130nm Technology

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Abstract— **One of the many applications of CMOS technology is the design the temperature sensors. In this paper, the electrical performance of smart CMOS(Si and 4H-SiC) temperature sensor in 130 nm technology have been studied using OrCAD PSpice software. The proposed CMOS circuit is developed to provide the first smart temperature sensor based on two different semiconductor technologies (Si and 4H-SiC) integrated on the same chip. These technologies are activated separately according to the temperature range (Low and High). The study of this smart sensor have shown that they operate under a low voltage less than 0.8 V and ultra low power of order nW. In addition, it is characterized by high sensitivity and good linearity across a temperature range from -120°C to 500°C. It is expected that the use of Si and 4H-SiC technologies for both temperature ranges (low and high) respectively will increase the life of this sensor.**

Keywords—Si; 4H-SiC; Temperature; Smart Sensor; CMOS

I. INTRODUCTION

Naturally, all semiconductors physical parameters are related to temperature change. That's why all designs and feasibility studies of semiconductor devices have to take into account normal working temperature range [1]. For this, temperature sensors play an important role in many measurement and in different fields of electrical engineering [2]. With the fast evolution of science and technology, the need of high performance, High and fast processing, low power consumption and small chip. Furthermore, high accuracy is required for the temperature sensors [3]. For this, the smart temperature sensor was invented in recent years [4]. So that it is considered an integrated system that consists of a temperature sensor, processor and interface electronics [5]. The linearity, sensitivity, temperature range and low power consumption are among the most important characteristics of the sensor [2].

The MOS transistors in Silicon technology have been shown to be more optimal for CMOS circuit design due to the improved subthreshold slope and the reduced leakage current compared to bulk CMOS [6]. In addition, many semiconductors have been proposed to replace Si technology, among these materials Silicon Carbide (SiC) (3C-SiC, 4H-SiC and 6H-SiC), this is due to their distinctive properties such as wide bandgap, high saturation velocity of electrons and high thermal conductivity [7].

In this paper, we will study the electrical behavior of smart CMOS(Si and 4H-SiC) temperature sensor in 130 nm technology. Based on the MOSFETs transistors in Si and 4H-SiC technologies by BSIM3v3 Model [6-7], we propose a new smart temperature sensor design integrated these technologies in a one-chip. Then we simulate this smart sensor with a supply voltage of 0.8V and in the temperature range – 120 to 500 °C.

II. SMART CMOS TEMPERATURE SENSOR DESCRIPTION

A block diagram of the proposed smart CMOS(Si and 4H-SiC) temperature sensor is shown in Fig. 1. Each block is a sub-circuit of overall circuit of sensor. Current source sub-circuit (transistors M1 to M5 in Fig. 2) is a self-biasing circuit which generates a current independent of bias voltage. Two temperature variation sub-circuits, these sub-circuits consist of three pairs of transistors (transistors M6 to M14 and transistors M15 to M23 for the Si and 4H-SiC technologies respectively) operating in sub-threshold region and connected in series as shown in Figure 2. They are directly biased with current mirror formed by PMOSi transistors. In this circuit, output voltage is proportional to temperature change if MOSi and MOS(4H-SiC) transistors drain current I_D varies exponentially with gate-source voltage V_{GS} (Eq.3). Calibration sub-circuit is two NMOSi transistors (M_{Cal1} and M_{Cal2}) point used to calibrate temperature sensor from a reference voltage (voltage calibration V_{Cal}).

Control sub-circuit is a programmable logic circuit which allows one of two temperature variation sub-circuits to be activated by the switches (Φ and $\overline{\Phi}$ of Fig.1, transistors MOSFETs MSw(Si) and MSw(4H-SiC) of Fig.2), because these switches are connected between the temperature variation sub-circuits and the current source sub-circuit and the calibration sub-circuit.

The circuit operation can be understood from the block diagram of Fig. 1 and the simulation circuit of Fig.2. When the temperature is below 140°C (low temperature range), the output of the control sub-circuit is set to a logic "1 0" which turns the switch (Φ) on for the temperature variation sub-circuit in Si technology. When the temperature becomes over 140°C (high temperature range), the output of the control sub-circuit is switched and turns on the second switch ($\bar{\Phi}$) of the temperature variation sub-circuit in 4H-SiC technology.

The drain current in sub-threshold region of a MOSFET is given by Eq.1 [8]:

$$I_D = KI_0 \exp\left(\frac{V_{GS}-V_{Th}}{nV_T}\right).\left(1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (1)$$

Where:

$$I_0 = \mu_{eff}\sqrt{\frac{q\varepsilon_{SiGe}N_{ch}}{2\Phi_s}}{V_T}^2 = \mu_{eff}C_{ox}(\eta-1){V_T}^2 \quad (2)$$

V_T: Is thermal voltage,
K :Is geometric channel report
η :Is sub-threshold coefficient.

When V_{DS} is very low, the drain current I_D becomes almost independent of V_{DS} and given by:

$$I_D = KI_0 \exp\left(\frac{V_{GS}-V_{Th}}{nV_T}\right) \quad (3)$$

The output voltage V_{Out} of this smart CMOS(Si and 4H-SiC) temperature sensor can be expressed as :

$$V_{Out} = \begin{cases} \left(\frac{\eta_{Si}K_B}{q}\ln(6)\right)T + \Delta V_{Th-Si} & T < 140°C \\ \left(\frac{\eta_{4H-SiC}K_B}{q}\ln(6)\right)T + \Delta V_{Th(4H-SiC)} & T > 140°C \end{cases} \quad (4)$$

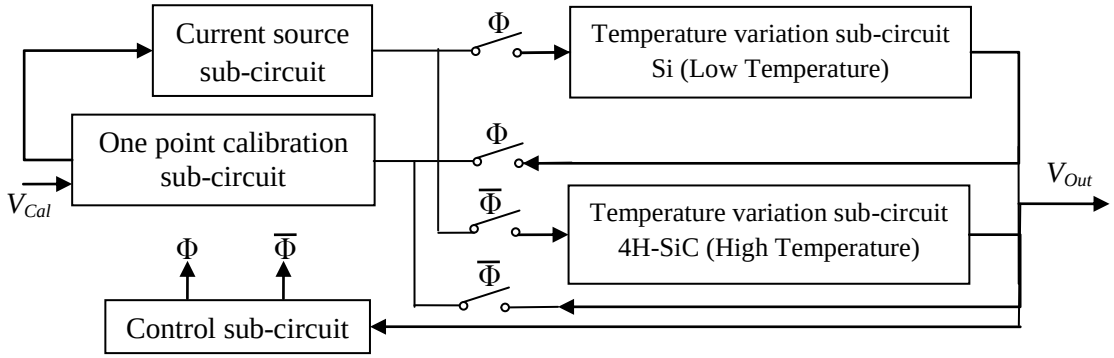

Fig.1. Block diagram of the proposed smart CMOS(Si and 4H-SiC) temperature sensor.

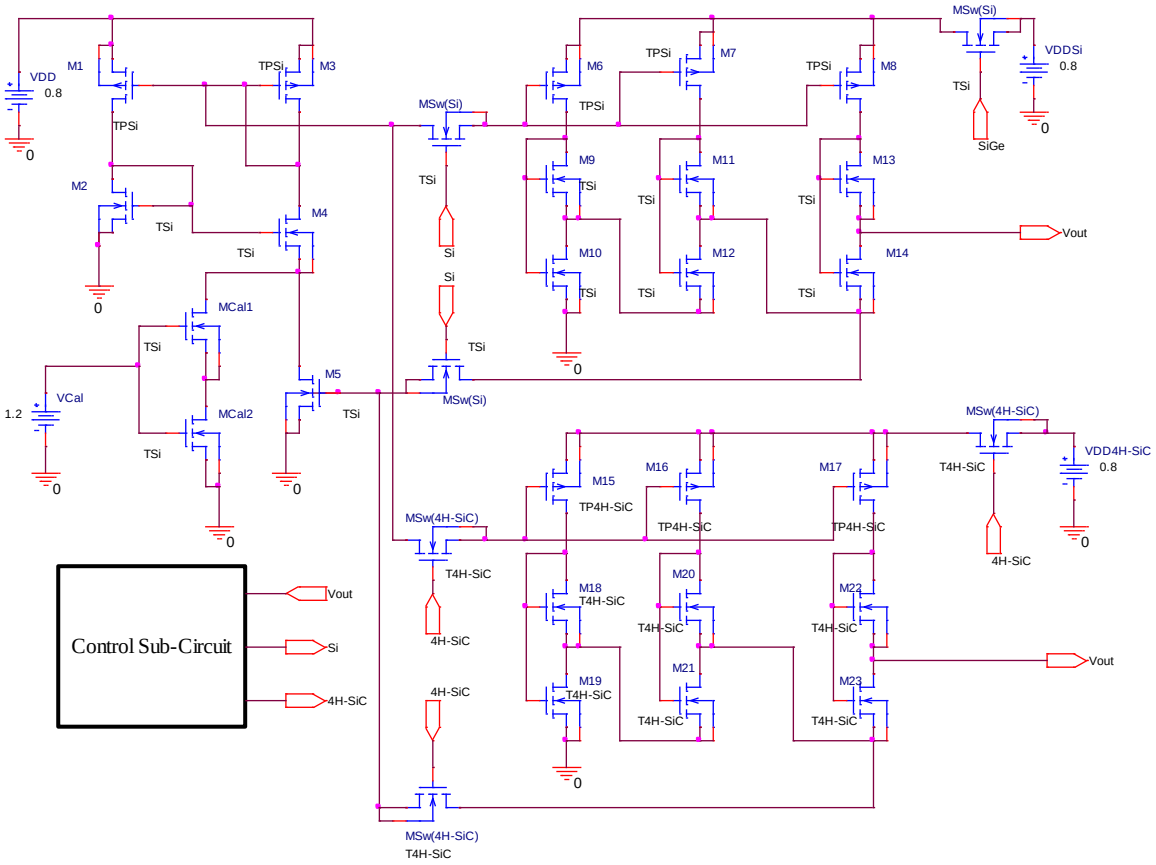

Fig.2. Smart CMOS(Si and 4H-SiC) temperature sensor simulation circuit.

III. RESULTS AND DISCUSSION

Fig.3. shows smart CMOS(Si and 4H-SiC) temperature sensor's output voltage simulation results as a function of temperature for both operating modes. As shown, sensor's output voltage V_{Out} is a linear function of temperature in different temperature ranges (Low and High) as expected from Eq. (4). The results obtained clearly show that the smart CMOS(Si and 4H-SiC) temperature sensor in 130nm technology works correctly according to the circuit operation proposed in this study.

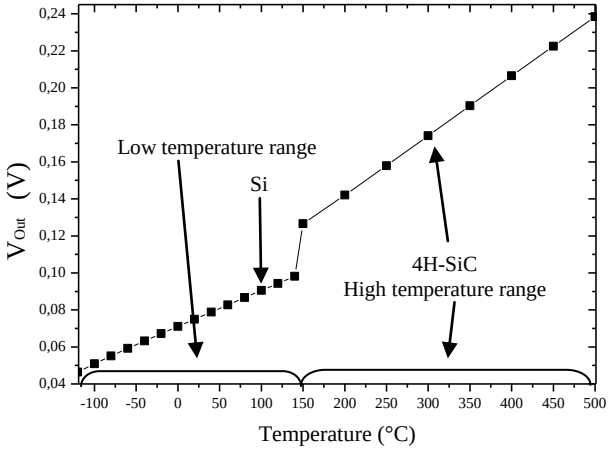

Fig.3. V_{Out} of smart CMOS(Si and 4H-SiC) temperature sensor.

The evolution of the output voltage V_{Out} as a function of the temperature in Fig.1 shows that this study achieves the good linearity of the smart CMOS(Si and 4H-SiC) temperature sensor in the both temperature ranges. The slope of this smart sensor is dependent on the threshold coefficient (η) in both temperature ranges (low and high) which distinguishes each type of semiconductor. This makes this smart sensor characterized by high sensitivity despite the high temperature, due to the transition from temperature variation sub-circuit in Si to temperature variation sub-circuit in 4H-SiC, which correspond to the two temperature ranges low and high respectively as shown in Table I. The different properties illustrated in Table I show that the smart sensor is characterized by an ultra low power due to the circuit of this smart sensor operates in sub-threshold region and that the transistors of this sensor proved their worth in the low power [6-7]. The transition between the two temperature variation sub-circuits according to the temperature allows for an increase in the life of this smart sensor. The results show that the smart CMOS(Si and 4H-SiC) sensor in 130nm technology is characterized by high electrical performace in a large temperature range.

TABLE I. PROPERTIES OF THE SMART CMOS(Si and 4H-SiC) TEMPERATURE SENSOR.

Mode switches Parameters	**$\Phi = 1$ and $\bar{\Phi} = 0$**	**$\Phi = 0$ and $\bar{\Phi} = 1$**
Material	Si	4H-SiC
Sensitivity (mV/°C)	0.31919	0.3619
Consumption (nW)	39.1552 (at 120°C)	
Ranges (I and II) °C	-120 −140	140 −500
Range (°C)	-120 − 500°C	
Bias voltage (V)	0.8	
CMOS Technology (nm)	130	

IV. CONCLUSION

In this work, we investigated the integration of two semiconductors technologies (Si and 4H-SiC) in a CMOS smart temperature sensor. By studying a new smart CMOS(Si and 4H-SiC) temperature sensor in 130nm technology under Pspice BSIM3v3. Output voltage was found to change linearly with temperature. When powered with supply voltage 0.8 V, the smart temperature sensor has low power consumption. It has also been demonstrated that this smart sensor can be used in two temperature ranges with two different semiconductors technologies.

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